Application Note

Power Diode Reverse Recovery Simulation

Updated 2020.05

***Abstract*—This application note describes the use of the Crosslight NovaTCAD suite of simulation tools for the analysis and simulation of power diode transient reverse recovery (t_{rr}) phenomena. A simple P-i-N diode structure generated in CSUPREM is used to illustrate the behavior. The methodology is directly extended to the simulation of a high-voltage wide bandgap SiC Schottky diode as well. The analysis uses the mixed-mode feature of the APSYS simulation tool to illustrate diode behavior in a typical applications circuit.**

I. INTRODUCTION

Diode transient reverse recovery behavior is well-known to be a key contributor to the total energy losses in many power switching circuits [1-2]. When a p-n diode is in the conducting state, the voltage supporting region is flooded with minority carriers. This gives rise to conductivity modulation phenomena which results in low forward voltage drop. When the diode is abruptly switched from the on-state into the off-state these excess carriers must be removed before the diode is capable of blocking reverse voltage. This can result in a large transient reverse current leading to excess energy losses in power switching circuits.

The reverse recovery transient is determined by both conduction and recombination mechanisms which are influenced by the internal structure of the diode, carrier lifetime control techniques, direct circuit behavior and circuit parasitics. Fast and accurate TCAD analysis is crucial to properly understand these interactions and to enable optimized device design.

This application note presents template files useful for the analysis and optimization of power diode reverse recovery behavior using the Crosslight NovaTCAD framework. CSUPREM is used to generate the device structure from a simplified process sequence. This is imported into the APSYS device simulator for the electrical simulations. Template files for simulating transient reverse recovery behavior using the mixed-mode feature of the APSYS simulator are provided.

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II. REVERSE RECOVERY CHARACTERIZATION

The diode transient reverse recovery (t_{rr}) characteristics are simulated using the RLC test circuit of Fig. 1.

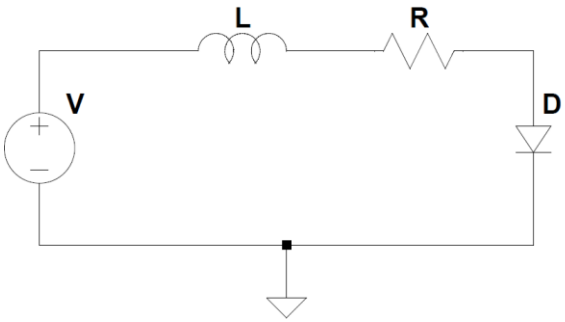

Fig. 1 Test circuit for t_{rr} simulation

To initiate the simulation the device is initially biased into the off-state at voltage $-V_r$. The input voltage is then switched to V_f. The current through the diode rises to a predetermined value at which point the diode is abruptly reverse biased to a voltage $-V_r$. The current falls at a constant ramp rate determined by the applied voltage and inductance.

$$\frac{di}{dt} = -\frac{V_r}{L} \qquad (1)$$

A typical reverse recovery waveform is shown in Fig. 2.

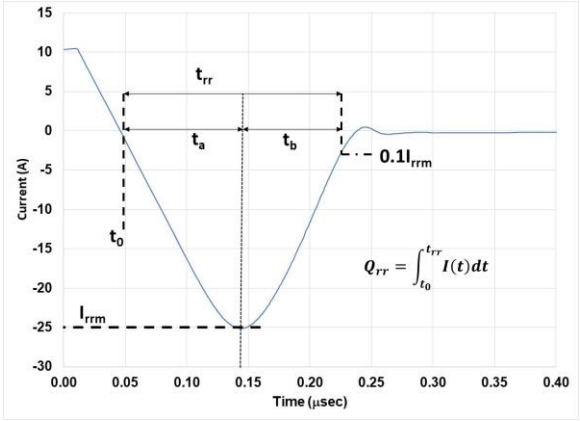

Fig 2. Typical reverse recovery waveform

III. REVERSE RECOVERY SIMULATION

A.) Process Simulation

The CSUPREM template file is used to generate the P-i-N diode used to illustrate the reverse recovery simulation. The resulting dopant profile is shown in Fig. 3.

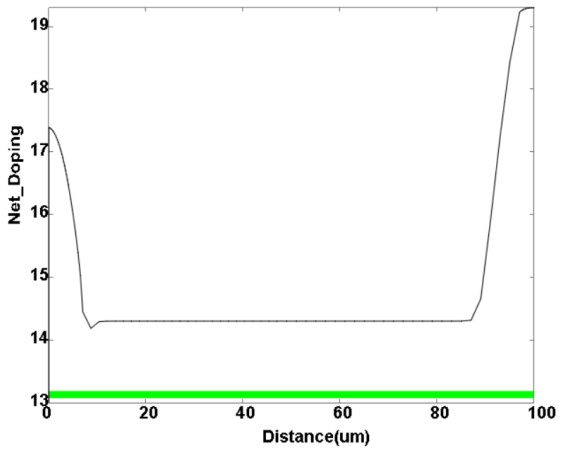

Fig 3. Typical P-i-N dopant profile

The p+ doping at the anode contact is $2.5x10^{17}$ cm^{-3} with a junction depth of nominally 8μm. The drift region is 80μm in length with a doping of $2x10^{14}cm^{-3}$. The n+ substrate has a doping of $2x10^{19}cm^{-3}$.

B.) Device Simulation

The device simulation uses the mixed-mode feature of the APSYS TCAD tool. In this mode, the TCAD device is defined inside a SPICE circuit file using a placeholder element. The Drift-Diffusion model then replaces the usual SPICE compact model of the device during the full mixed-mode simulation. An example template file is provided.

The device model is imported from CSUPREM using the statement

```
load_mesh mesh_inf=diode.aps
suprem_import=yes
```

The appropriate SPICE netlist file is defined using the statement

```
minispice circuit_file=Qrr.cir
z_dim=1E6 &&
spice_device_to_tcadmesh=Zdiode
&&
contact1_to_spice_node=2 &&
contact2_to_spice_node=0
```

The statement `z_dim=1E6` is used in conjunction with the CSUPREM output file to define the device area which in this example is 0.1 cm^2.

Accurate simulation of the diode reverse recovery process requires appropriate choice of minority carrier lifetime. In the APSYS simulation these are specified by the statements

```
lifetime_n value=1e-6 mater=1
lifetime_p value=1e-6 mater=1
```

In these example files the hole and electron lifetimes are assumed to be equal although is not necessarily a requirement.

The current vs. time waveform for the example diode is plotted in Fig. 4 for four different values of carrier lifetime, which are equal to each other. The forward current of 10A corresponds to a current density of $100A/cm^2$. The reverse bias voltage is 300V. In the plot the timescales have been adjusted so that t=0 corresponds to the beginning of the turn-off transient.

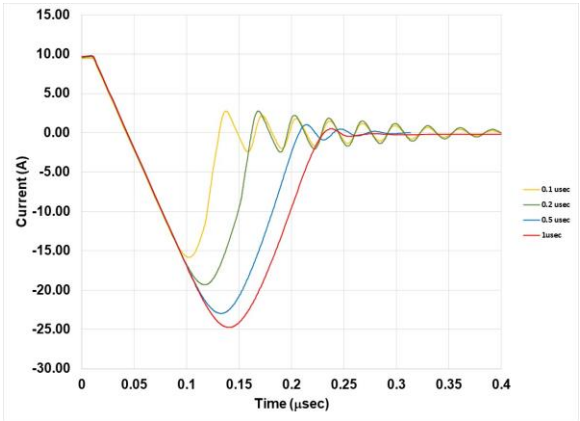

Fig 4. t_{rr} characteristics vs. carrier lifetime

The simulations show the reduction in peak reverse current (I_{rrm}) and reverse recovery time (t_{rr}) as the carrier lifetimes are decreased. The simulations also show that reduced carrier lifetime results in increased current overshoot and oscillatory behavior of the current waveform, commonly referred to as "snappy" recovery.

The simulation tools can be used to study the internal carrier dynamics of the diode as well as its time-dependent removal. Fig. 5 is an example of the minority-carrier concentration profiles at different time instances during the recovery process. These are obtained by capturing the APSYS output at the appropriate time intervals using the statement `print_step=0.01e-6`

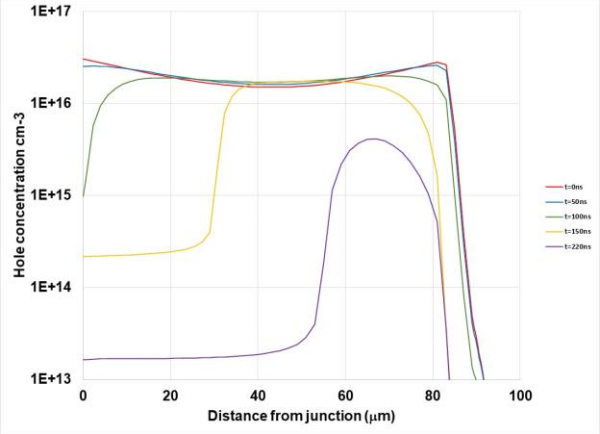

Fig 5. Hole concentration vs. time
Carrier lifetime=1 μsec

At time t=0 the minority carrier concentration is well above its equilibrium value due to the strong injection from the p+ anode. At t=50nsec the profile changes only slightly, indicating the diode is still forward biased. At t=100nsec the diode has begun to reverse bias and the hole concentration begins to drop near the p-n junction. As the time is increased beyond 100nsec the depletion region continues to spread into the n- region as seen in the figure.

The reverse recovery characteristics are also a function of the slope of the current transient (di/dt), as shown in Fig. 6. The plot shows that as di/dt increases, the maximum reverse current increases while the t_{rr} decreases. In the simulation di/dt is controlled by varying the value of the series inductance shown in Fig. 1.

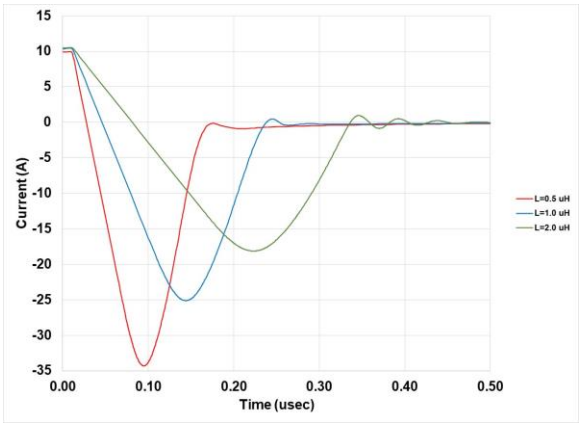

Fig 6. Reverse recovery as function of di/dt

Fig. 7 illustrates the use of the simulation tool to compare the reverse recovery characteristics of a 1200V SiC Schottky diode vs. a comparable silicon P-i-N structure. The simulated SiC structure consists of a 13μm thick epitaxial layer with n-type doping of $6.1x10^{15}cm^{-3}$ similar to that previously discussed [3]. The simulation shows the significantly reduced I_{rrm}, Q_{rr} and t_{rr} as would be expected for the SiC Schottky. This is due to the near complete elimination of minority carrier injection in the Schottky structure.

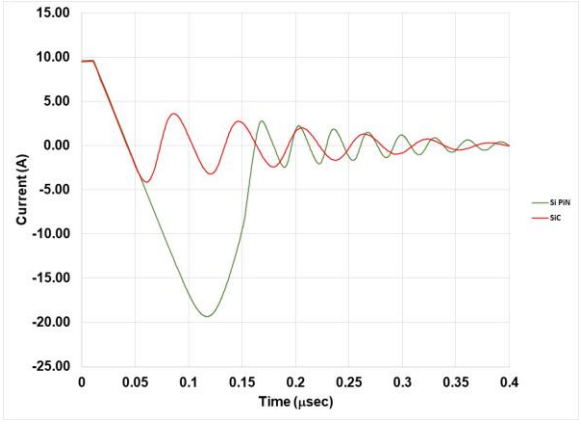

Fig. 7 Comparison of PiN reverse recovery vs. SiC Schottky

IV. SUMMARY

Template files for the simulation of diode transient recovery using the Crosslight NovaTCAD suite of simulation tools are provided. The examples illustrate the mixed-mode capability to analyze diode behavior. A methodology to simulate and optimize the key tradeoffs in diode switching speed has been demonstrated.

References

[1] J. Lutz et.al., “Semiconductor Power Devices-Physics,Characteristics, Reliability”, Springer International, (2011).

[2] B. J. Baliga, , “Fundamentals of Power Semiconductor Devices, 2nd Edition”, Springer, (2019).

[3] G. M. Dolny, “TCAD Files for SiC-JBS Demonstration”, Crosslight Software Inc. Application Note, (2016).