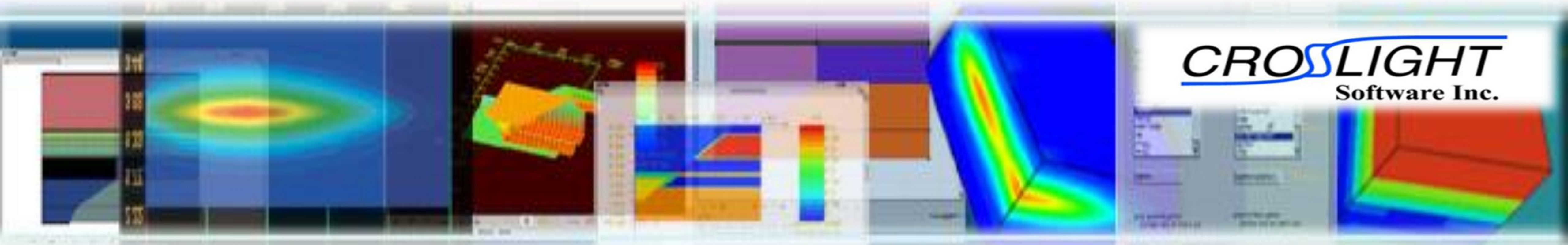

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Crosslight Simulation of Hysteresis Characteristics in Thin Film Transistors

CROSSLIGHT
Software Inc.

Contents

- Experiments
- Trap models
- Simulated structure and commands
- Results
- Process simulation
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Hysteresis found in both n-channel and p-channel TFT

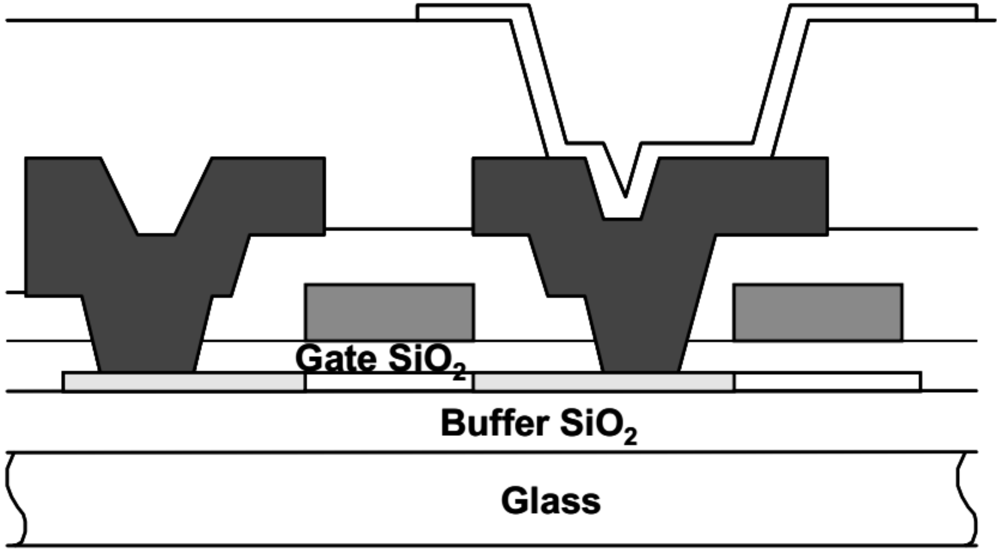


Fig. 1 Cross-sectional view of p-channel TFT

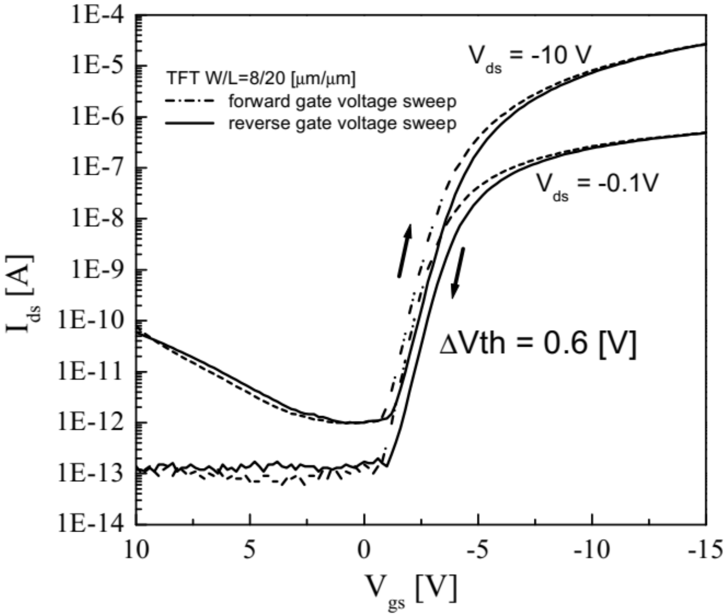


Fig. 2 Ids-Vgs characteristics of p-channel TFT

Improvement of Hysteresis Characteristics in p-channel Poly-Si TFTs

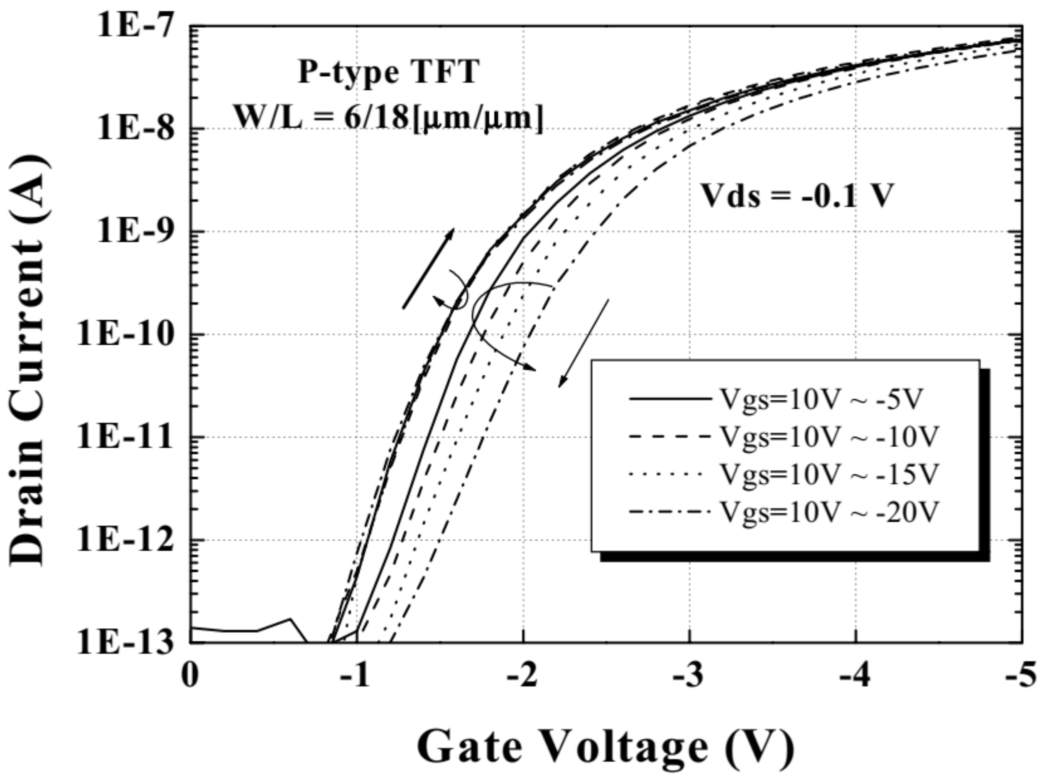
Byeong-Koo Kim, Ohyun Kim, Hoon-Ju Chung [1],
Sang-Gyu Kim [2], Chan-Il Park [2], Hong-Seok Choi [2],
and Yong-Min Ha [1]

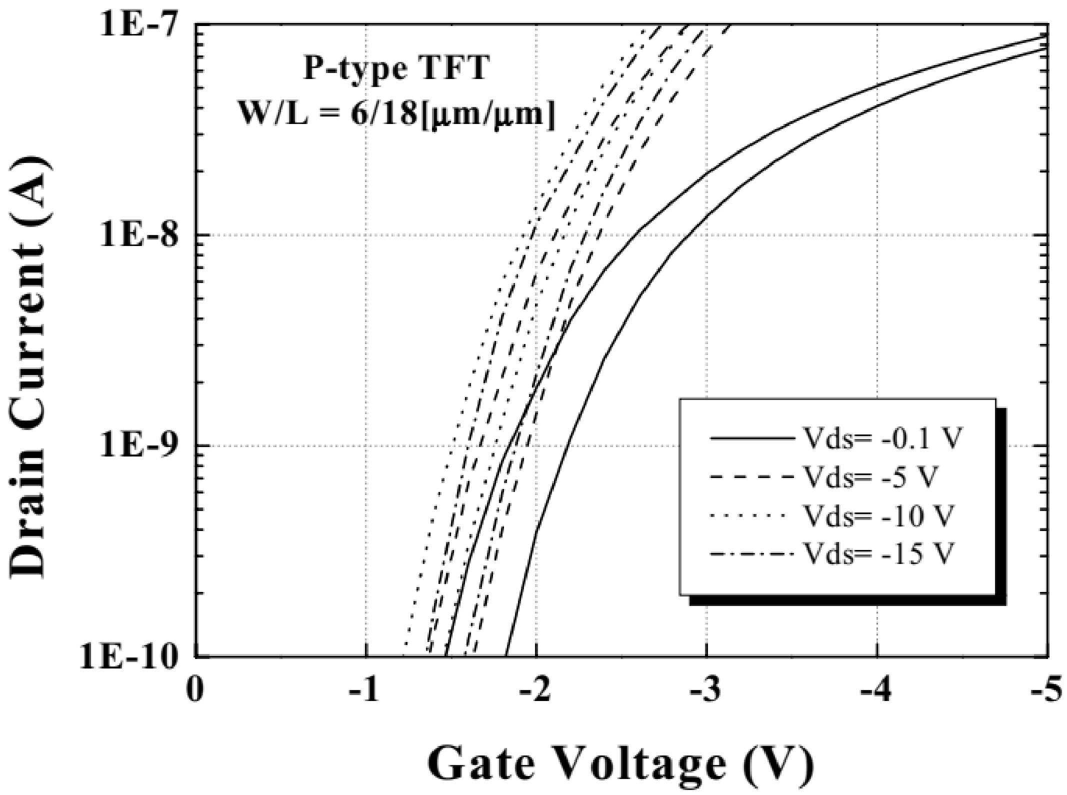
Hysteresis found in both n-channel and p-channel TFT

Journal of Information Display, vol. 6, no. 4, 2005

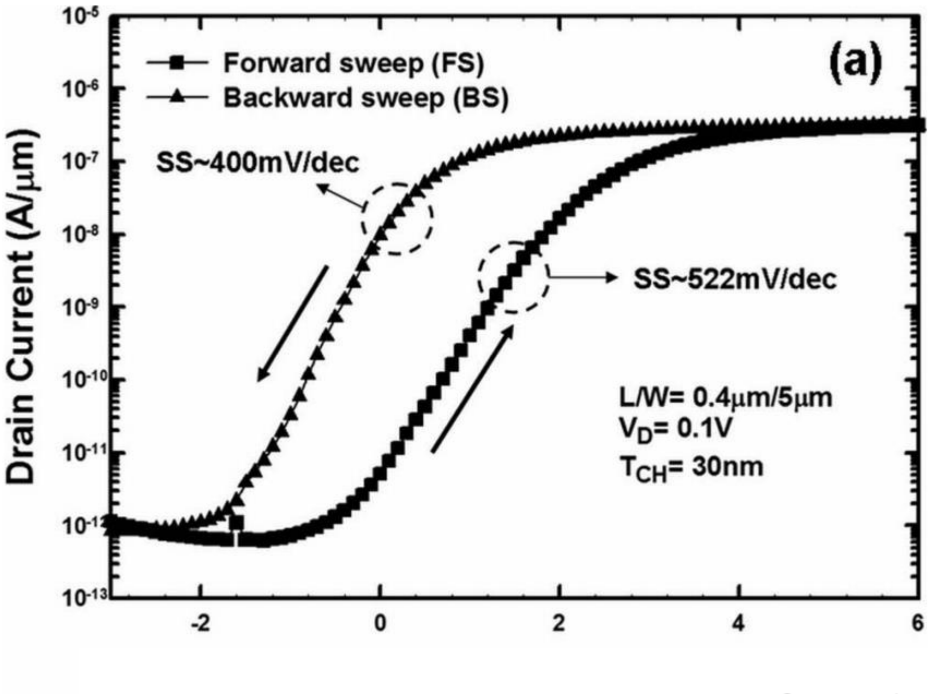
Hysteresis Characteristics in Low Temperature Poly-Si Thin Film Transistors

Hoon-Ju Chung[*a], Dae-Hwan Kim[b], and Byeong-Koo Kim[*b]





Hysteresis found in both n-channel and p-channel TFT



Deep level traps were identified as being the cause of hysteresis

JOURNAL OF APPLIED PHYSICS **105**, 054502 (2009)

Origin of hysteresis in current-voltage characteristics of polycrystalline silicon thin-film transistors

Horng-Chih Lin,[1,2,a)] Cheng-Hsiung Hung,[2] Wei-Chen Chen,[2] Zer-Ming Lin,[2]
Hsing-Hui Hsu,[2] and Tiao-Yuang Hunag[2]

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Trap Dynamic Model

$$-\nabla\cdot\left(\frac{\epsilon_0\epsilon_{dc}}{q}\nabla V\right) = -n + p + N_D(1-f_D) - N_A f_A + \sum_j N_{tj}(\delta_j - f_{tj}),$$

$$\nabla\cdot J_n - \sum_j R_n^{tj} - R_{sp} - R_{st} - R_{au} + G_{opt}(t) = \frac{\partial n}{\partial t} + N_D\frac{\partial f_D}{\partial t},$$

$$\nabla\cdot J_p + \sum_j R_p^{tj} + R_{sp} + R_{st} + R_{au} - G_{opt}(t) = -\frac{\partial p}{\partial t} + N_A\frac{\partial f_A}{\partial t}.$$

$$R_n^{tj} = c_{nj} n N_{tj}(1 - f_{tj}) - c_{nj} n_{1j} N_{tj} f_{tj}$$

$$R_p^{tj} = c_{pj} p N_{tj} f_{tj} - c_{pj} p_{1j} N_{tj}(1 - f_{tj})$$

Traps affect both the space charge and current continuity, and they can be very slow (some deep traps take days to recover since the trapping rates are small)

$$N_{tj}\frac{\partial f_{tj}}{\partial t} = R_n^{tj} - R_p^{tj}$$

Trapping and detrapping

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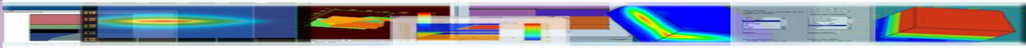

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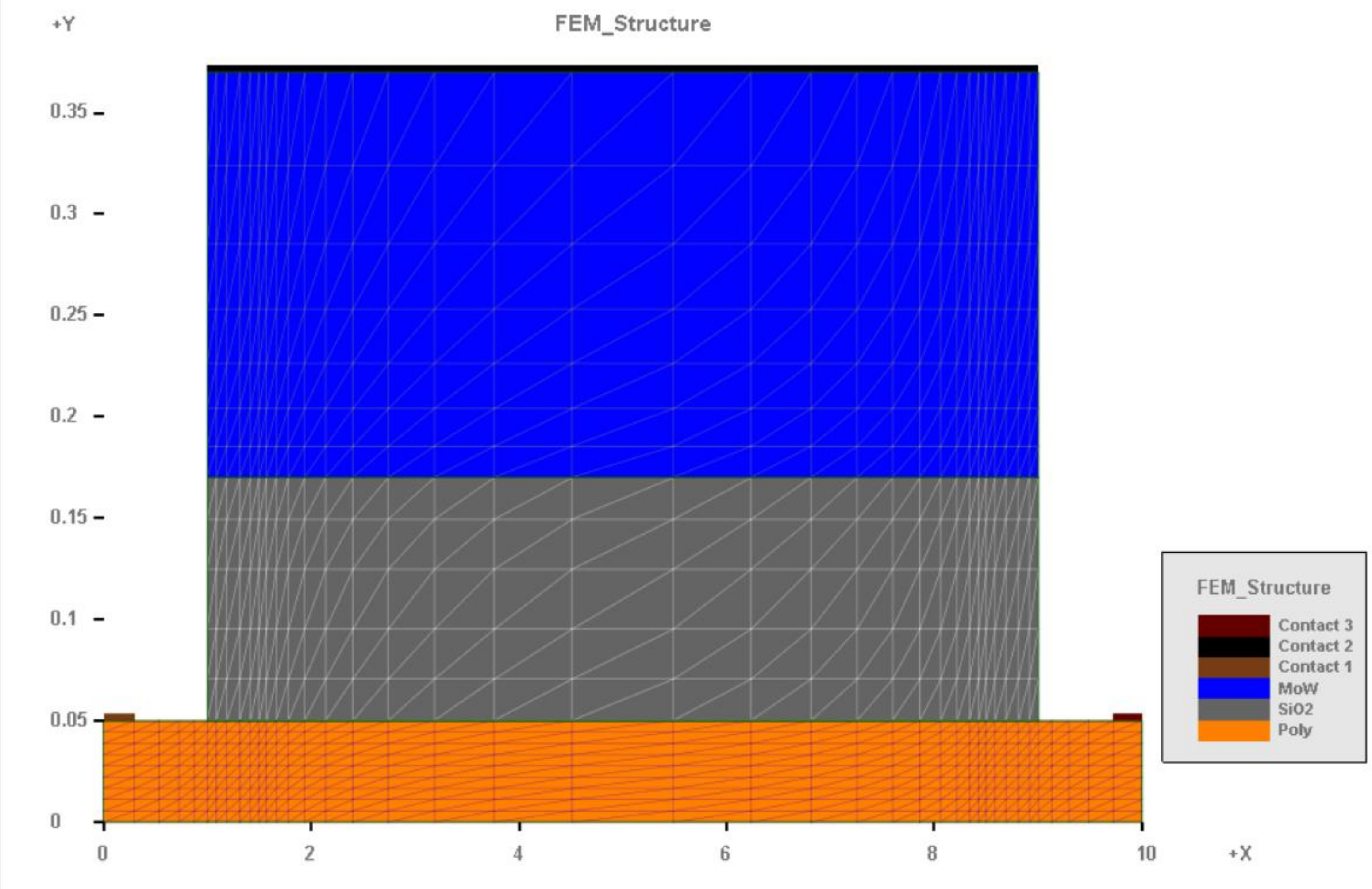
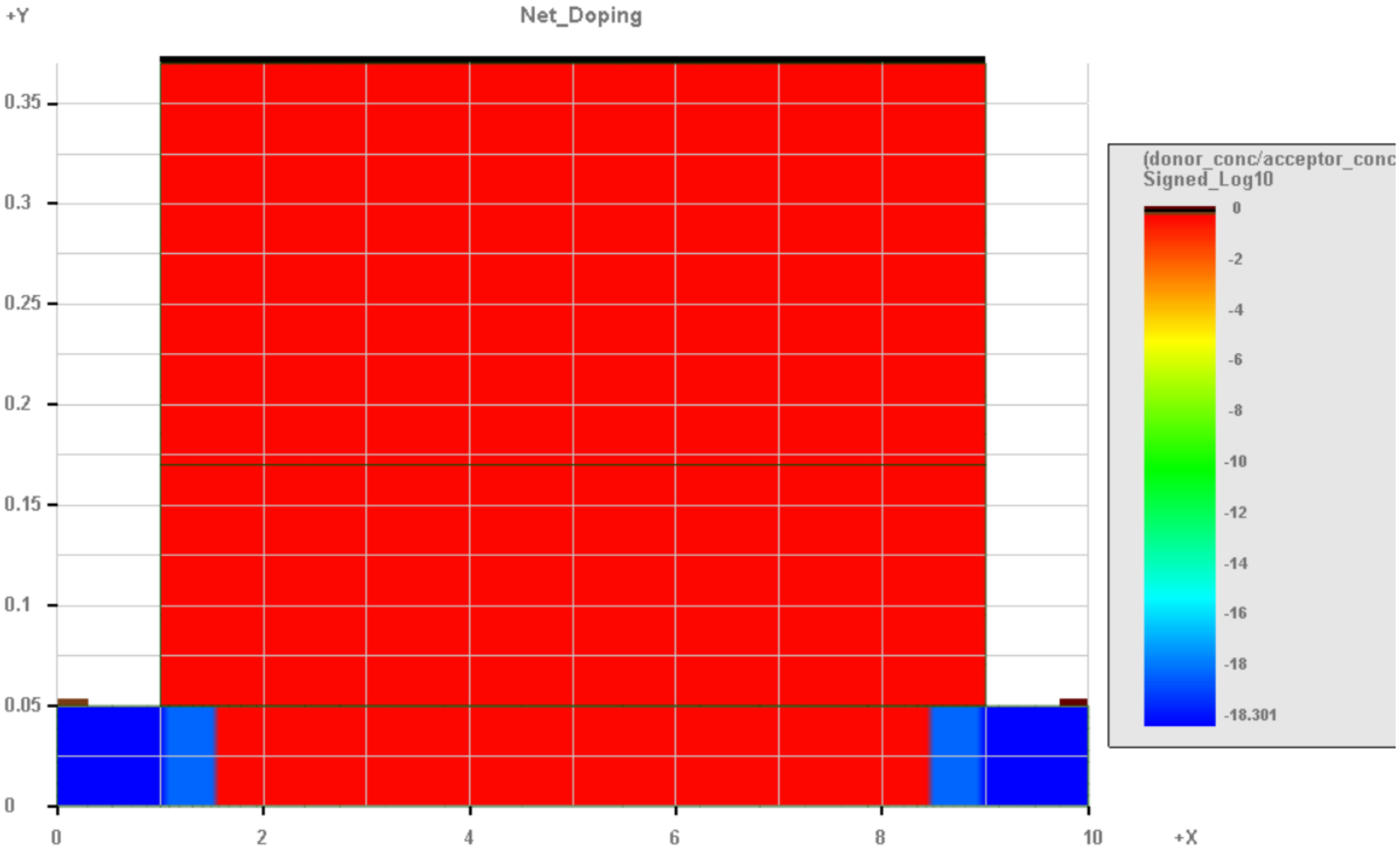
Simplified p-channel TFT



Initial net-doping as defined in LayerBuilder



Definition of deep level traps

```
doping impurity=trap_2 charge_type=donor level=0.65
max_conc=2.e23 &&
x_prof=(0   20.  0.1 0.1) y_prof=(0   10.  0.1 0.1)
trap_ncap_2 value=1.e-23 mater=1
trap_pcap_2  value=1.e-23 mater=1
```

- Trap level calculated from the conduction band edge.
- Use of trap_2 instead of trap_1 since trap_1 is reserved for the usual carrier lifetime setting.
- Ncap or pcap refers to carrier trapping interaction cross section in m^2. In plain words, carriers interact/scatter with the trap/defect with such this cross section. It should be on the order of or less than the trap/defect area. (nm squared or less).
- Uniform single discrete level trap is the most simple form of carrier trapping while providing well defined space charge. More complicated forms include interface traps and trap with continuous energy level distributions. Crosslight provides a strong and physical TCAD platform for various deep traps.
- Deep level traps originate from crystal defects and are sensitive to growth process conditions

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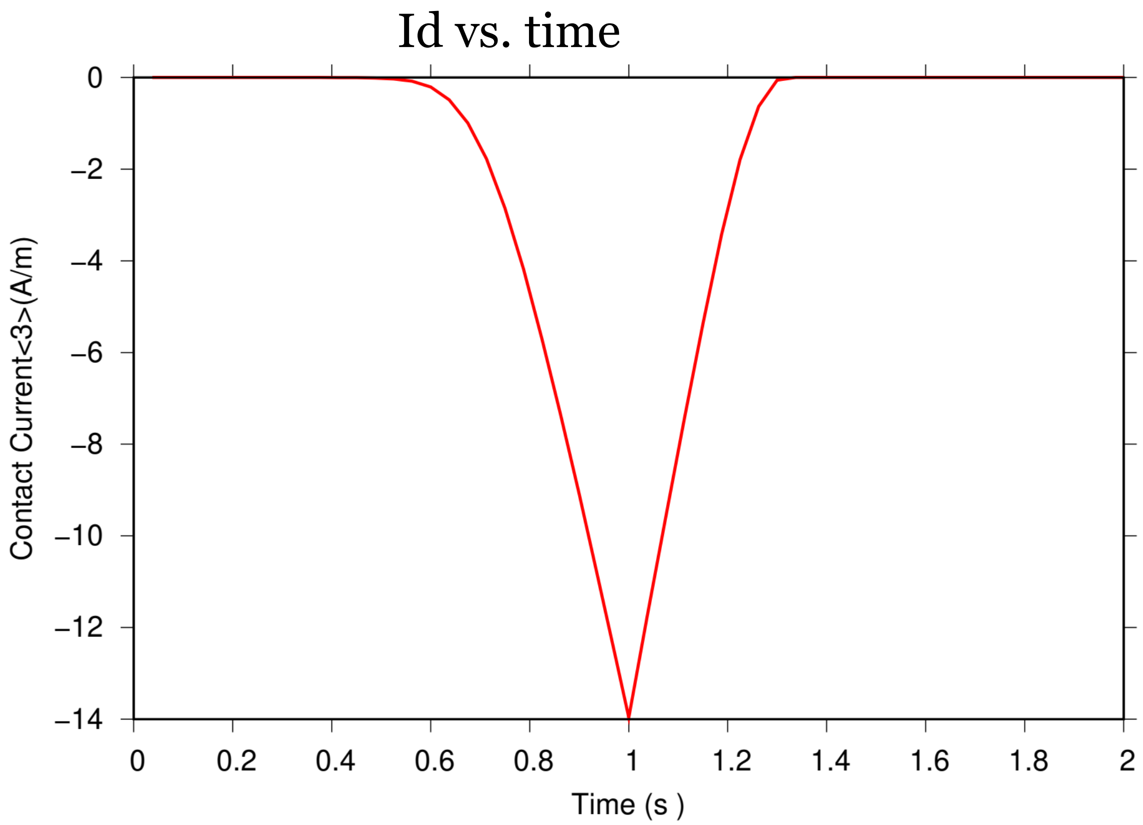
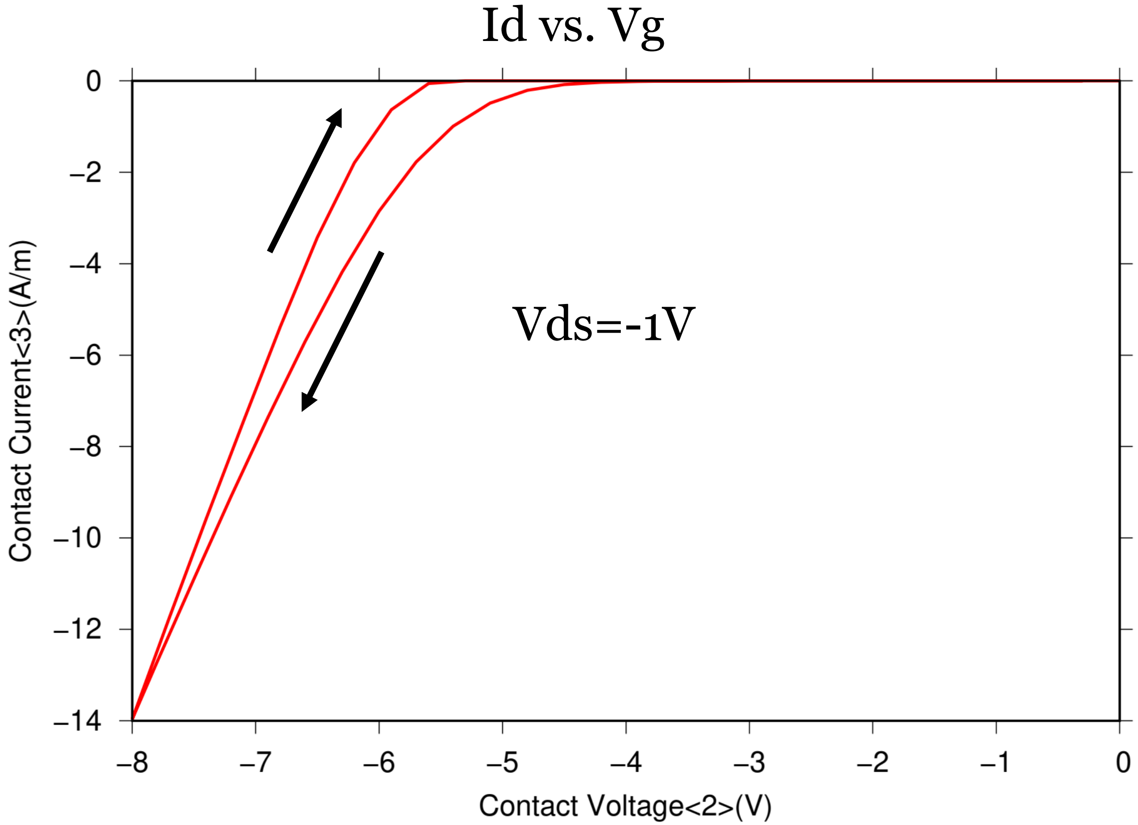
Turn on/off characteristics with hysteresis





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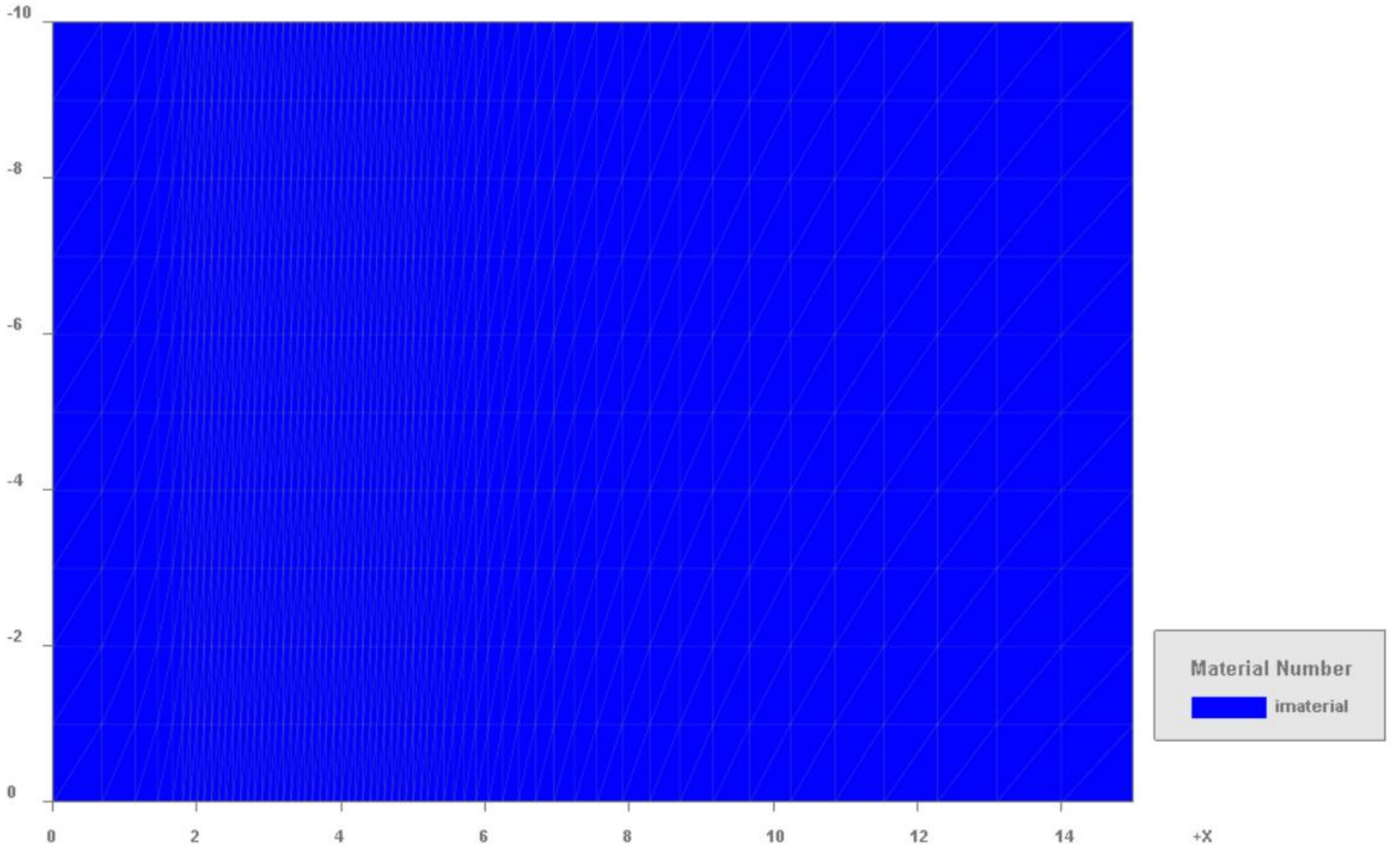
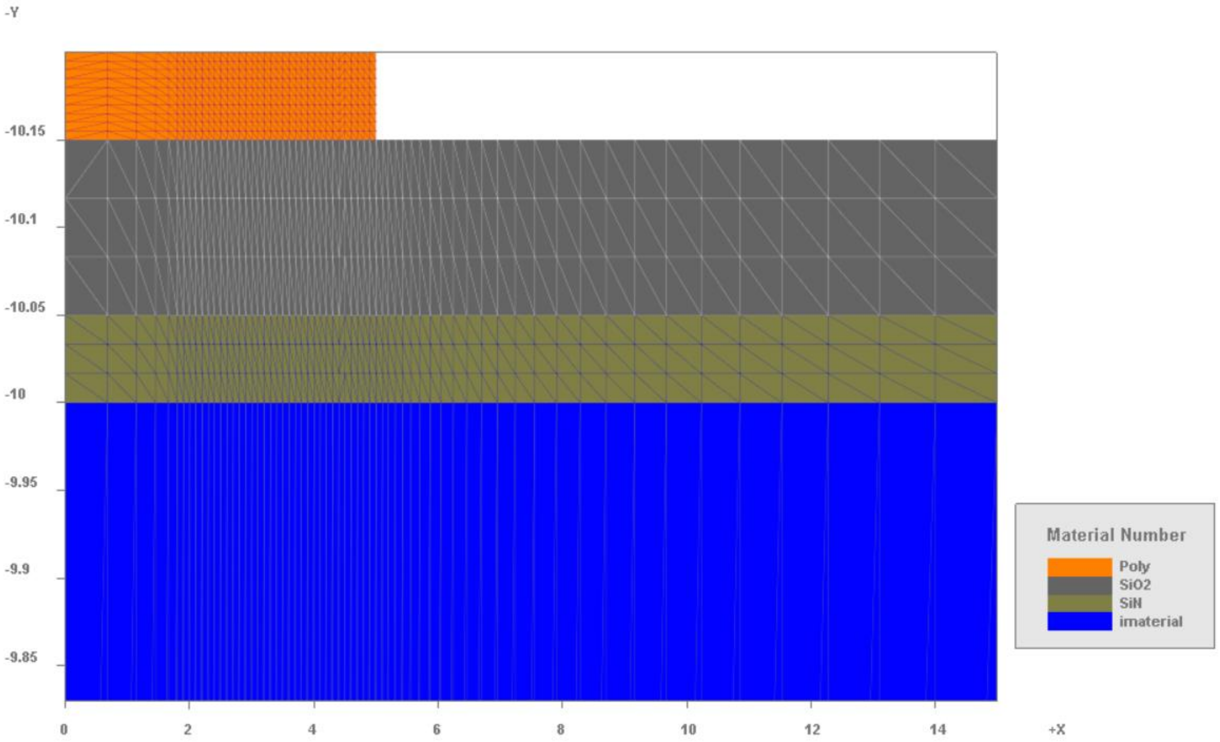
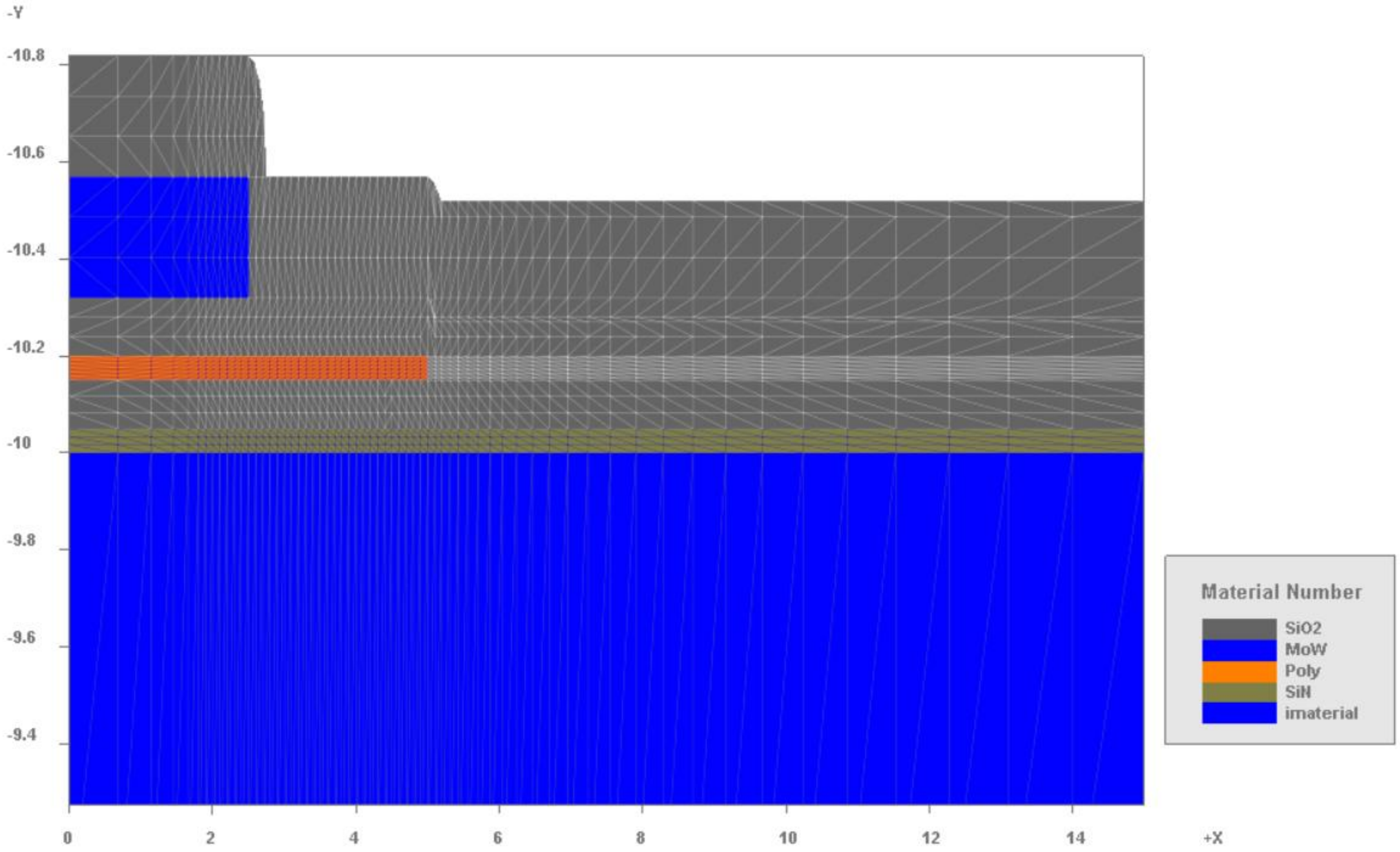
```
region imaterial xlo=lft xhi=rht ylo=top yhi=bot
bound exposed xlo=lft xhi=rht ylo=top yhi=top
bound backside xlo=lft xhi=rht ylo=bot yhi=bot

init
struct outf=01_sub.str
```



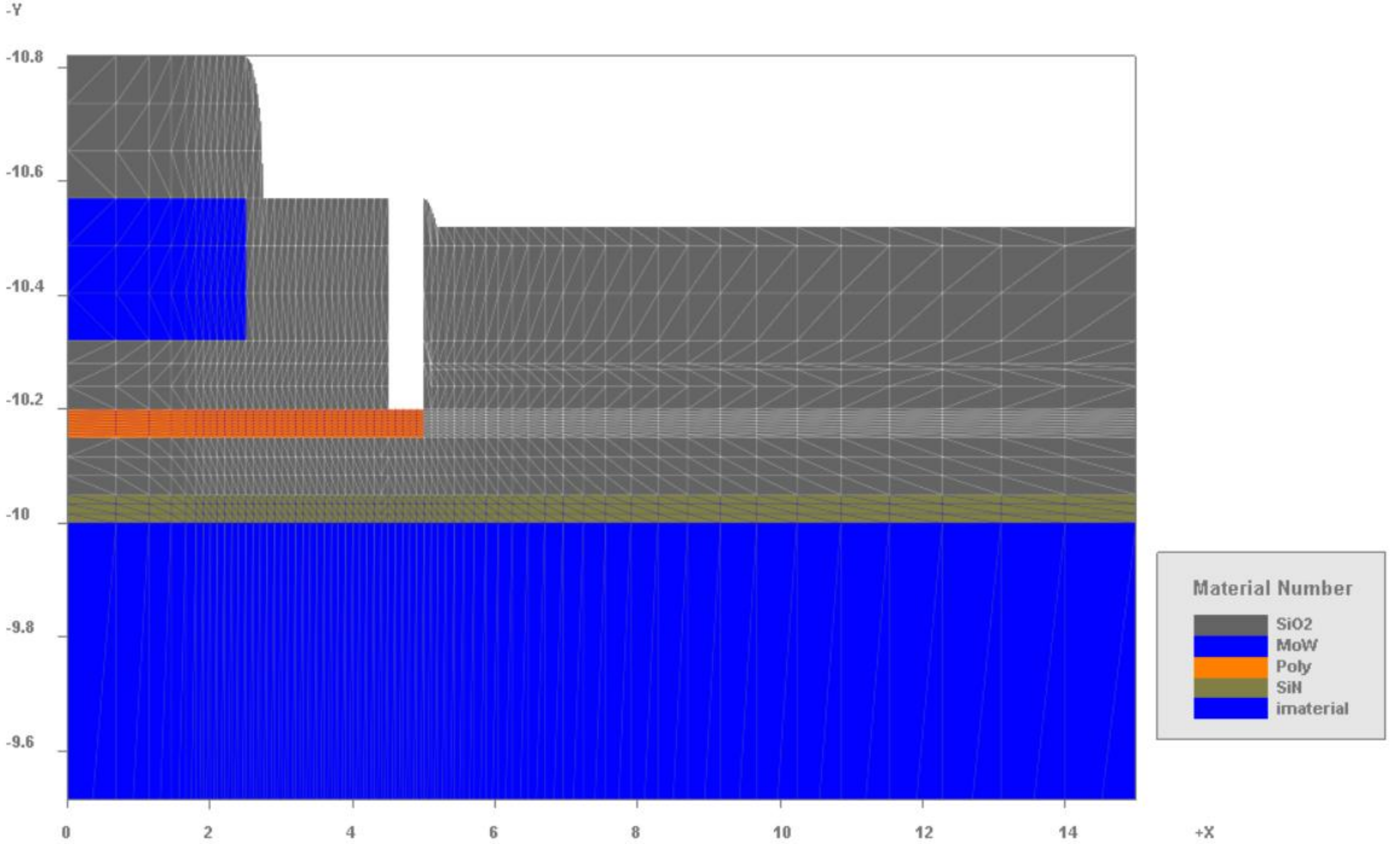
```
#2_gate-iso
deposit nitride thick=0.05   meshlayer=3
deposit oxide thick=0.1   meshlayer=3

# deposit the gate poly
deposit poly phosphorus conc=1.0e17 thick=0.05
meshlayer=10

#4_source_drain_elec
mask thick=1. x1.from=0.0 x1.to=2.0  x2.from=5.0
x2.to=15.0
implant boron dose=1e13  energy=15
etch photoresist all

etch poly  p1.x=5 right

#anneal
diffuse time=5 temp=450

struct outf=02_ACT.str
```



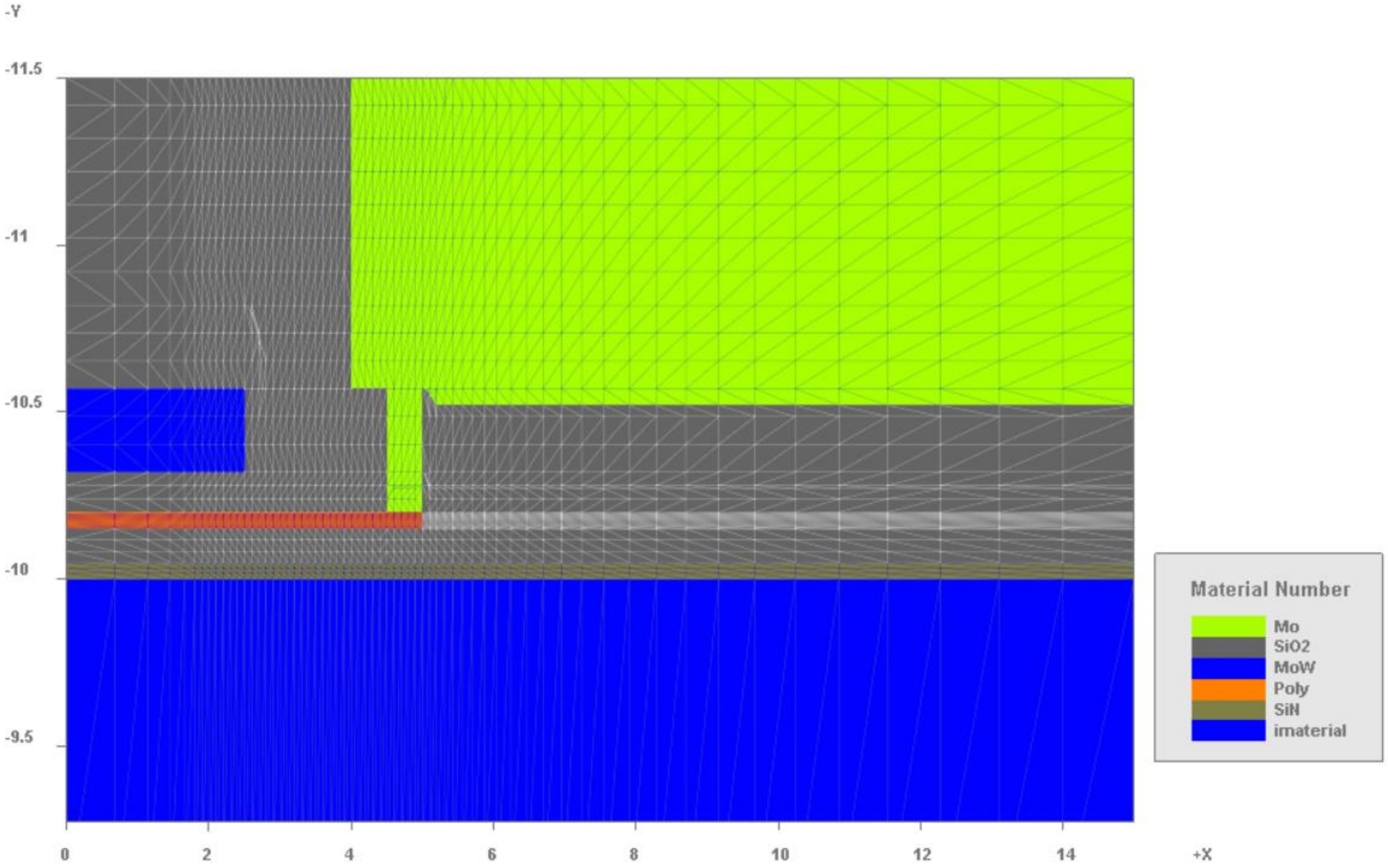
```
#3_gate_elec
deposit oxide thick=0.12   meshlayer=3
deposit MoW thick=0.25   meshlayer=3
etch    MoW p1.x=2.5  right

deposit oxide thick=0.25   meshlayer=3

struct outf=03_gate_elec.str
```



```
#4_source_drain_elec
mask thick=1. x1.from=0.0 x1.to=4.50  x2.from=5.0 x2.to=15.0
etch oxide  avoidmask depth=1
etch photoresist all

struct outf=04_source_drain_elec_1.str
```

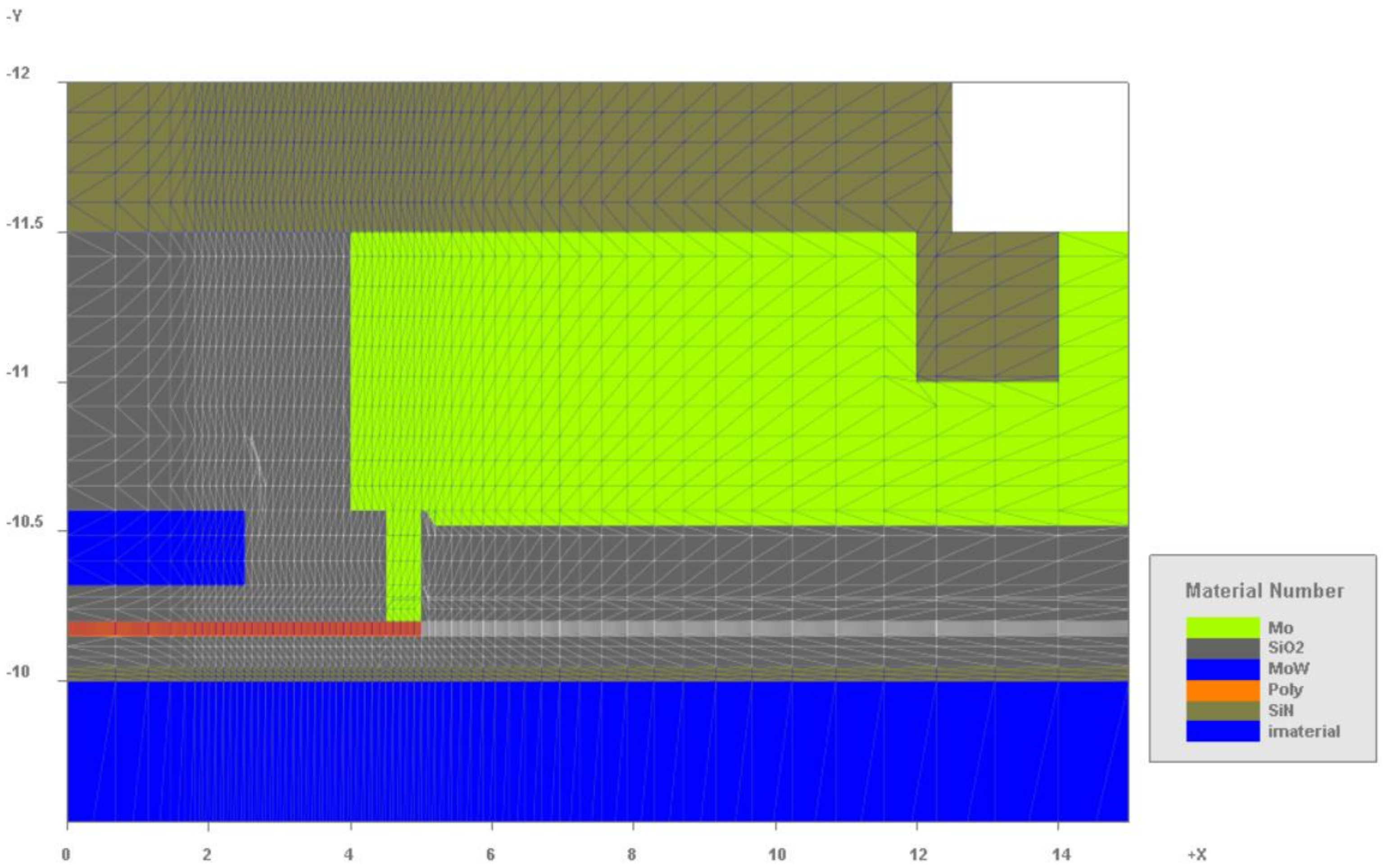


```
deposit Mo  thick=1.0 meshlayer=10
etch Mo p1.x=4.0  left

deposit oxide thick=1.0  meshlayer=10

cmp  y=-11.5 above

struct outf=04_source_drain_elec.str
```

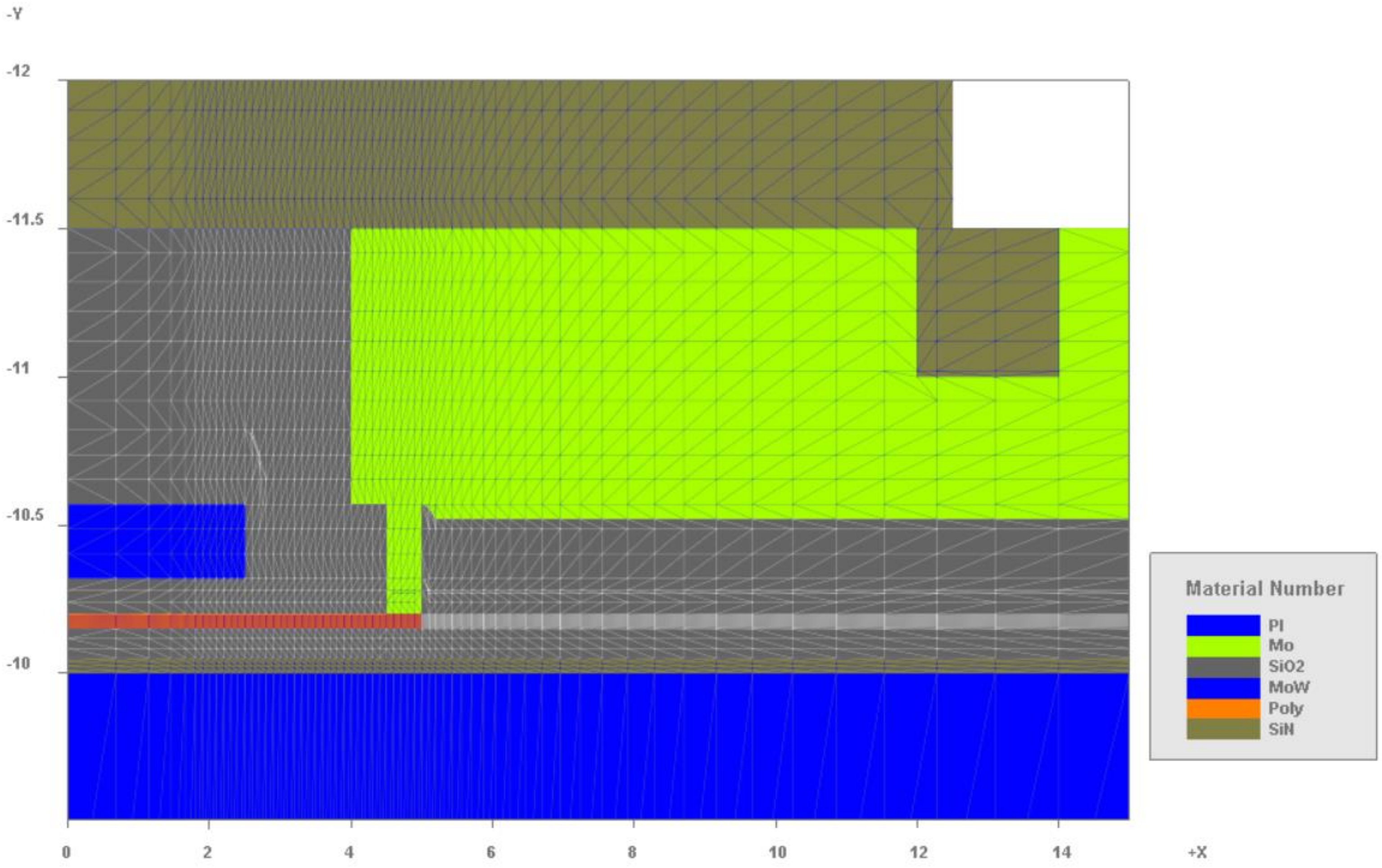


#5-top_nitride

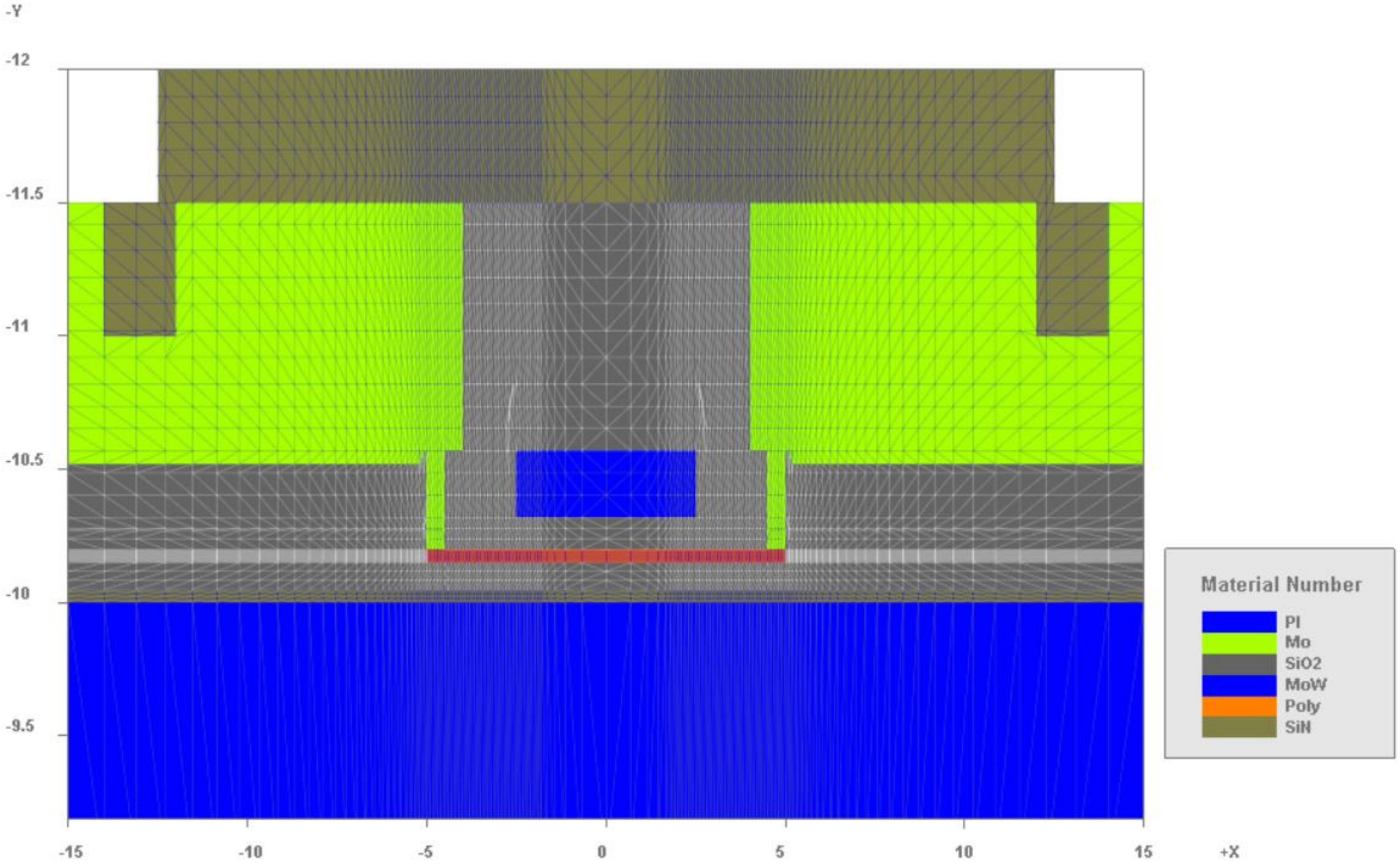
```
mask thick=1. x1.from=0.0 x1.to=12.0  x2.from=14.0
x2.to=15.0
etch Mo  avoidmask depth=0.5
etch photoresist all

deposit nitride thick=1.0  meshlayer=10
cmp  y=-12.0 above

mask thick=1. x1.from=0.0 x1.to=12.5
etch nitride  avoidmask depth=0.5
etch photoresist all

struct outf=05_top_nitride.str
```

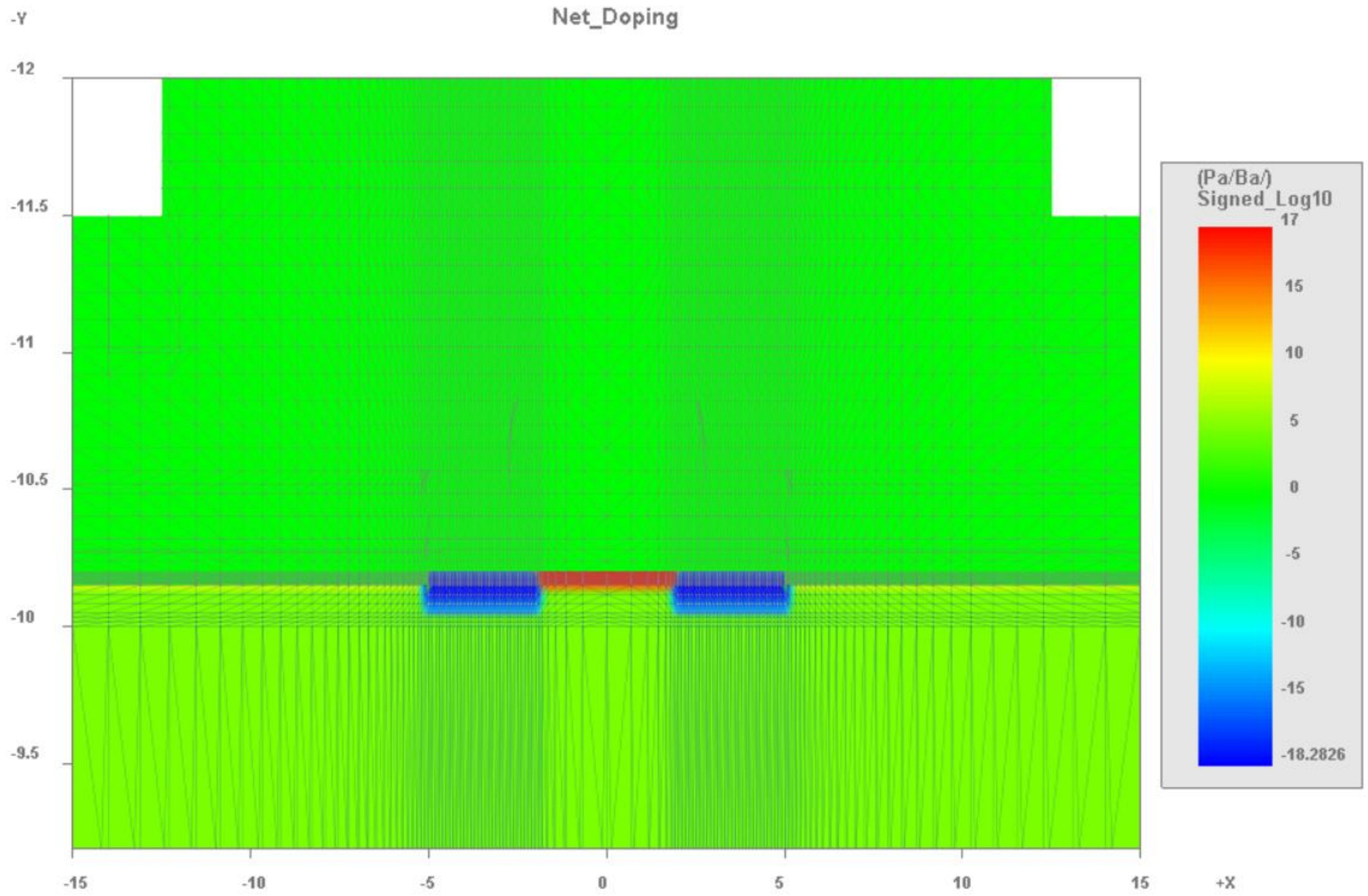


```
change_material  imaterial  /PI  file=PI.txt

struct outf=06_PI.str
```



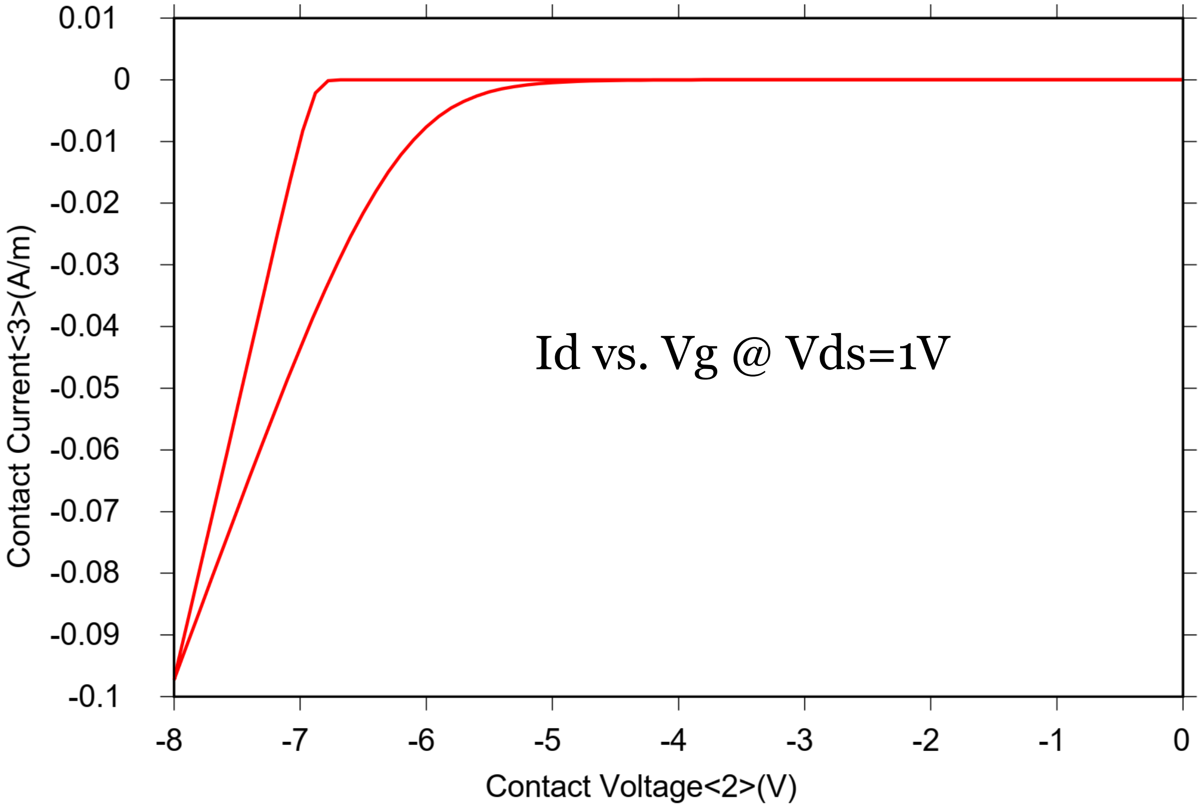
```
# reflect the structure
struct mirror left

struct outf=07_final.str
```




Net_Doping
-Y
-12
-11.5
-11
-10.5
-10
-9.5
-15
-10
-5
0
5
10
15
+X
(Pa/Ba/)
Signed_Log10
17
15
10
5
0
-5
-10
-15
-18.2826

```
doping impurity=trap_2 charge_type=donor level=0.65
max_conc=2.e23 &&
x_prof=(-15.   15.  0.1 0.1) y_prof=(0   15.  0.1 0.1)
trap_ncap_2  value=1.e-23 mater=4
trap_pcap_2  value=1.e-23 mater=4
```

For device simulation, add deep-level traps in its most simple form: single level, uniformly distributed mid-gap donor traps



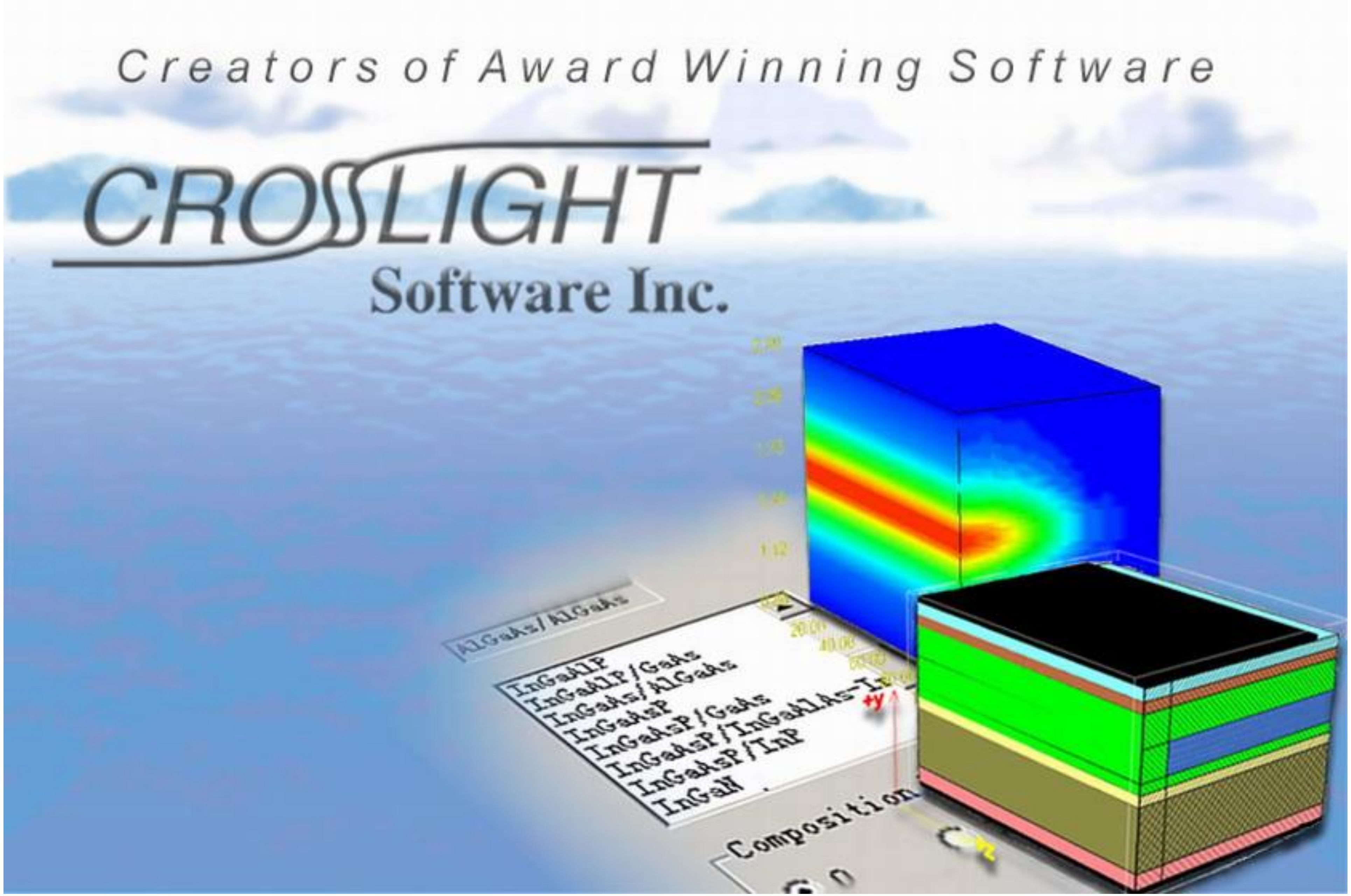
Summary

- Crosslight provides advanced deep level trap model for TFT (LTPS, IGZO or a-Si)

- Experimental trends can easily be reproduced

- Useful for resolving processing/design issues in research or production

Thanks for your attention!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InGaAs/AlGaAs
InGaAsP
InGaAsP/GaAs
InGaAsP/InGaAlAs-In
InGaAsP/InP
InGaN
+y
Composition