



Application Note

Silicon Superjunction MOSFET Simulation

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Abstract--A technology template for the simulation of silicon superjunction MOS power transistors using the Crosslight NOVATCAD suite of simulation tools is provided. The example illustrates the use of the process simulation tool CSUPREM to generate the basic device structure. This structure is then imported into the device simulator APSYS for the electrical simulations. A methodology to simulate the superjunction MOS electrical characteristics including the drain breakdown voltage, on-state resistance, junction capacitances and gate charge is demonstrated. Simulation results are displayed and analyzed using the CrosslightView plotting tool.

I. INTRODUCTION

Over the past several years silicon superjunction (SJ) power MOSFETs have gained broad commercial acceptance and have become the device of choice for 600V-class applications. In contrast to the uniformly doped drift region of conventional power MOSFETs, a superjunction drift region comprises alternating pillars of N-type and P-type dopant with approximately equal net charge. In the off state, the alternating regions are mutually depleted. If this depletion occurs at a voltage below that which causes the critical electric field to be reached, the drift region is able to support high voltage. Moreover, since the pillars can be made relatively narrow, it is possible to greatly increase the allowed charge in the conducting layers of the drift region, which provides significantly reduced on-state resistance. In order to properly understand and optimize these devices fast and accurate TCAD modeling is essential. This application note presents template files useful for the analysis, design and optimization of superjunction power MOSFET devices using the Crosslight NOVATCAD framework. CSUPREM is used to generate the device structure from the basic process sequence. This is imported into the APSYS device simulator for the electrical simulations. Template files for simulating device on-resistance, drain breakdown voltage (BV_{dss}) gate charge and capacitances are provided.

Fig. 1. shows a cross-section of the unit cell of a typical 600V superjunction MOSFET [1].

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The device is formed in a n-type epitaxial drift layer on a n+ substrate. Under charge-balanced conditions the epitaxial layer thickness t_{epi} is determined by the desired breakdown voltage according to

$$E_{cr}t_{epi} = BV \quad (1)$$

where E_{cr} is the critical electric field for breakdown. The p-type columns are formed from a deep trench and epitaxial-refill process. The widths and doping concentrations of the n- and p-pillars are adjusted to satisfy the charge balance condition

$$N_d W_n = N_a W_p \quad (2)$$

where N_d , N_a are n-column and p-column doping concentrations and W_n , W_p and the n- and p-pillar widths respectively.

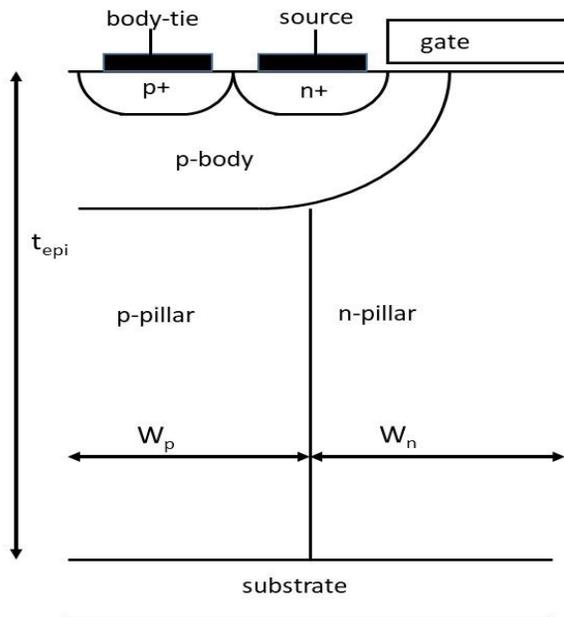


Fig. 1 Schematic Cross Section of Superjunction MOSFET

II. PROCESS SIMULATION

The process simulation represents a generic SJ transistor similar to the device described in [1]. The breakdown voltage is designed to be in the

650V range. The details of the process simulation are given in the template files.

The key process steps simulated are outlined below.

- 1.) N-epitaxial growth
- 2.) Deep trench etch and refill
- 3.) Gate oxidation
- 4.) Polysilicon gate deposition
- 5.) P-body implant and drive in
- 6.) Source implantation and anneal
- 7.) Body contact implantation and anneal
- 8.) Contact formation

The initial set of CSUPREM statements

```
define @Wp 3.0
define @Wn 3.0
define @Tepi 32
define @Nd 3.3E15
define @Na 3.3E15
```

specify the values of the important device parameters defined above. Additional device dimensions are calculated internally based on these basic definitions to simplify parametric optimization studies.

A n-type epitaxial layer is initially defined with thickness of @Tepi and concentration of @Nd. This is followed by a deep, anisotropic trench etch followed by a p-type epitaxial trench fill. A simulated CMP process follows to planarize the wafer surface. A simple thermal oxidation grows a nominally 60 nm oxide in a dry oxygen ambient. Furnace ramp rates and partial pressure oxidations which are commonly used in commercial process flows are ignored, but can easily be added if desired.

Next the gate polysilicon is deposited with simulated in-situ doping and then patterned. The p-body region is formed from a boron ion implantation and drive-in step to form the channel region. The n+ source region is patterned and implanted, followed by the p+ body tie region. A thermal drive-in activates the dopants and sets the final junction depths and channel length. Finally, any remaining oxide is removed in regions which will form the electrical

contacts. The full simulation structure is shown in Fig. 2, while Fig. 3 shows a close-up of the surface channel region. The lateral doping profile along the surface is shown in Fig. 4.

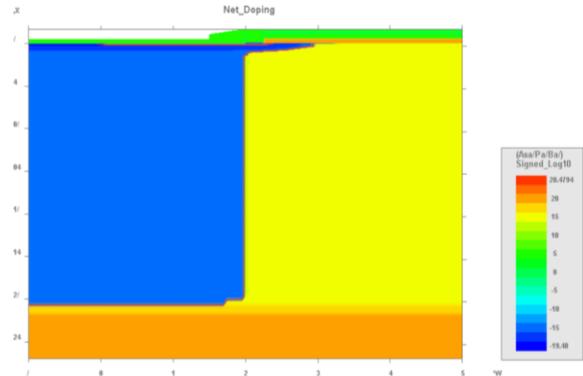


Fig. 2 Simulation Cross Section of Superjunction MOSFET

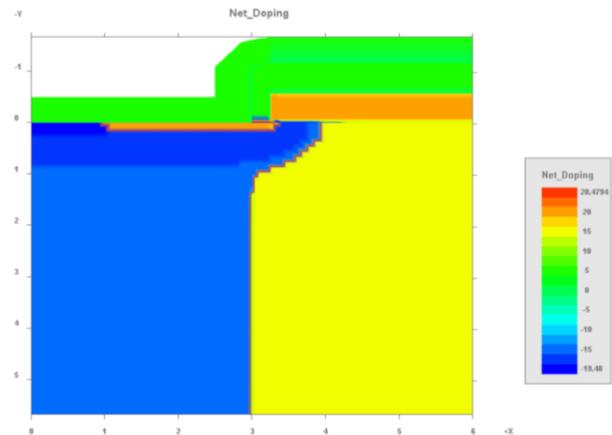


Fig. 3 Surface channel region

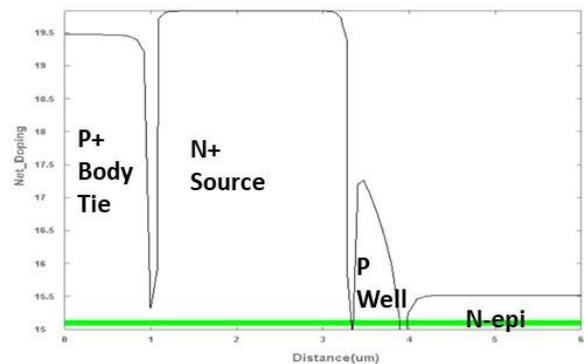


Fig. 4 Channel doping profile for SJ MOSFET example

III. DEVICE SIMULATION

The device electrical characteristics are simulated using the APSYS 2-dimensional finite element device simulation tool. Unless otherwise specified the APSYS default physical models are used in these simulations. Complete listings of the APSYS input files are provided in the template files.

A. Simulation setup

The SJ device structure previously generated with the CSUPREM export statement is the input structure for the device simulations.

The `load_mesh` statement is used to enter the device structure into APSYS. The subsequent `suprem_to_apsys_material` commands map the CSUPREM materials into the APSYS materials. `suprem_mater` is the original material number in the CSUPREM file, which by default defines SiO₂ as material 1, SiN as material 2, Si as material 3, and polysilicon as material 4. `apsys_mater` is the corresponding material number in APSYS. The `load_macro` statements are used to describe the properties of the various materials used in the structure as defined in the materials database. The `suprem_contact` statements are used to define the electrodes on the mesh imported from the process simulator.

The `interface` statement is used to specify the oxide charge, in units of m^{-2} . The `mobility_xy` statement models the vertical field mobility reduction in the SJ channel using the Lombardi model while the `impact_chynoweth` input statement specifies the Chynoweth formulation and coefficients for impact ionization. The `set_minority_carrier_virtual_eg_kt = 31` statement plays no actual role in the simulation. It exists only to provide a fitting parameter which allows the users flexibility to match the simulated reverse leakage current to measured data.

The statement `newton_par` controls the

parameters of the Newton solver used in the software, which can be modified to improve convergence. The scan statements define the bias conditions on each electrode for the various electrical simulations.

B. BV Simulation

Device breakdown voltage characteristics are computed from the template file "SJ_BV.sol". The scan statements shown below.

```
scan var=voltage_3 value_to=2000
min_step=1e-6 max_step=10.0
auto_finish=current_3
auto_until=3e-8
auto_condition=above
init_step=0.001
```

```
scan var=current_3 value_to=1e-4
init_step=1.1e-8 min_step=1.e-9
max_step=1.e4
```

Initially the drain voltage is swept until a specified avalanche current is reached as defined by the `auto_finish` and `auto_until` statements. After this the simulation switches to a current boundary condition to allow the rest of the I-V curve to be computed. A typical I-V curve at breakdown is shown in Fig. 5, with a simulated breakdown voltage of 667V.

Fig. 6 plots the two-dimensional electrostatic potential at breakdown. The plot illustrates the well-known linear potential profile observed in ideally charge balanced SJ devices.

Fig 7 plots the electric field at breakdown both at the center of the p-pillar (green curve) and at the center of the n-pillar (blue curve). The field is mostly uniform but increases at the surface and the epi-interface respectively. This effect is further illustrated in Fig. 8, which plots the 3-dimensional electric field distribution. This figure also shows an increase in electric field at the p-pillar/n-pillar junction.

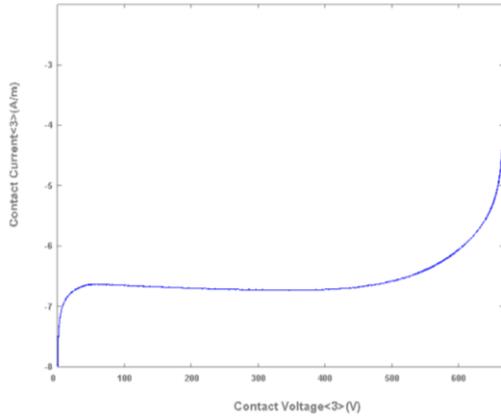


Fig 5. Simulated breakdown characteristic

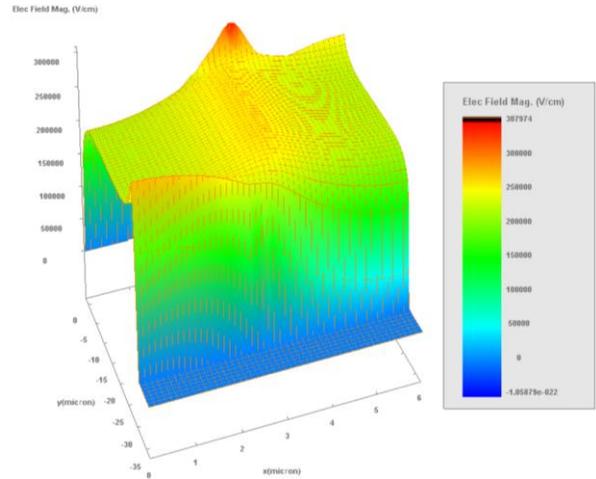


Fig 8. 3D electric field profile

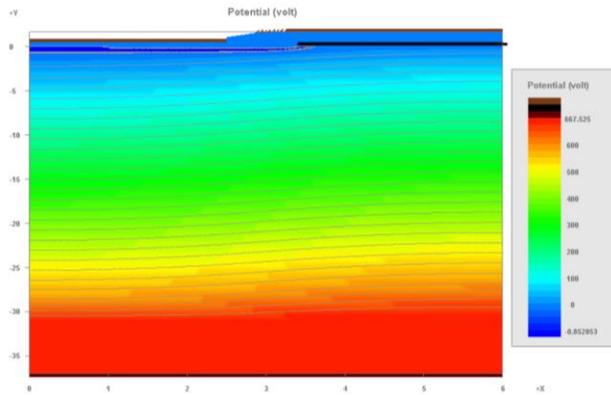


Fig 6. Simulated equipotential lines at breakdown

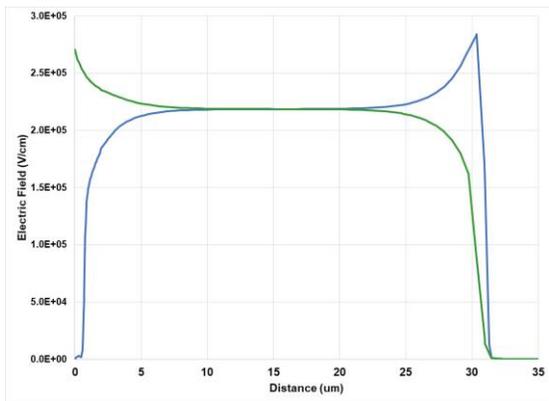


Fig 7. Simulated electric field profiles at center of p-pillar (green) and n-pillar (blue)

C. RdsOn Simulations

The on-state resistance is computed from the template file "SJ_Rds.sol". The scan statements are shown below.

```
scan var=voltage_2 value_to=5
min_step=1e-9 max_step=0.5 &&
init_step=0.001
```

```
scan var=voltage_3 value_to=2
min_step=1e-6 max_step=0.5 &&
init_step=0.001
```

```
scan var=voltage_3 value_to=0
min_step=1e-6 max_step=0.5 &&
init_step=0.001
```

```
scan var=voltage_2 value_to=10
min_step=1e-9 max_step=0.5 &&
init_step=0.001
```

```
scan var=voltage_3 value_to=2
min_step=1e-6 max_step=0.5 &&
init_step=0.001
```

The simulation calculates the I-V characteristic for two values of gate bias, 5 and 10 V. For each value of gate voltage, the drain voltage is swept from 0 to 2volts. After the 5V trace is completed, the drain voltage is swept back to zero volts before the gate potential is increased.

The $R_{ds(on)}$ data is shown in Fig. 9. The simulated $R_{ds(on)}$ of ~ 11 mohn-cm² at a current density of 100 A/cm² and gate voltage of 10V is typical of state-of-the-art commercial devices [2].

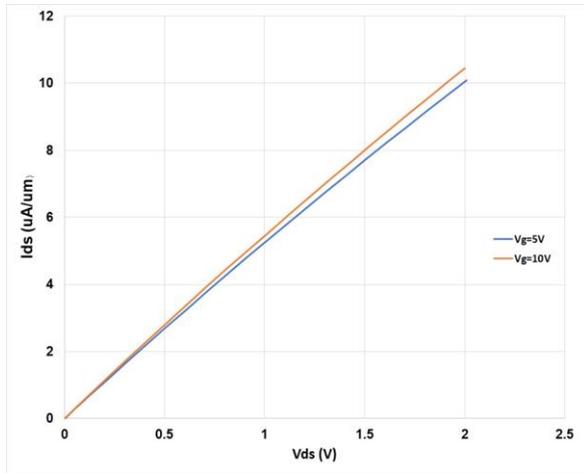


Fig 9. Simulated R_{ds} characteristic

D. Gate Transfer Characteristics

The gate transfer characteristics are computed from the template file “SJ_IdVg.sol”. The scan statements are shown below.

```
scan var=voltage_3 value_to=0.1
init_step=1.1e-8 min_step=1.e-9
max_step=0.05
```

```
scan var=voltage_2 value_to=10
init_step=1.1e-8 min_step=1.e-9
max_step=0.05
```

The drain voltage is set to 0.1V then the gate is swept from 0 to 10V. The characteristics are shown for two different ambient temperatures as shown in Fig. 10. The temperature is specified using the temperature temp=xxx statement where xxx is the desired ambient temperature in Kelvin. The threshold voltage can be estimated from the zero-current extrapolation of this plot. This value can vary slightly from the data sheet definition of threshold which is measured at a fixed current with $V_{gs}=V_{ds}$. The plot clearly illustrates the negative temperature coefficient of gate threshold voltage as well as the mobility

reduction with temperature evidenced by the reduced drive current at elevated temperature.

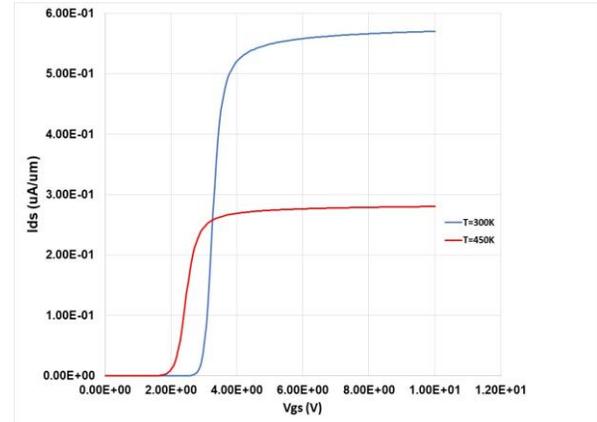


Fig 10 Gate transfer characteristics

E. Gate Charge Characteristics

The Superjunction MOSFET gate charge characteristics are simulated using the APSYS mixed-mode capability with the approach described in [3]. The main APSYS solution is done from the template file “SJ_Qg.sol”. The associated circuit file for mixed mode analysis is the template Qg_netlist.cir. The 2-dimensional device structure from CSUPREM is first loaded using the statement load_mesh mesh_inf=sj_mos.ap suprem_import=yes. The structure is then scaled to an active area of 0.1 cm² in the third dimension using the statement 3d_solution_method skip_fv_data=yes z_structure single_plane_zdim=1.66e6

The active device is then specified for mixed-mode analysis using the statements minispice circuit_file=Qg_netlist.cir && spice_device_to_tcadmesh=SJ_MOS && contact1_to_spice_node=0 && contact2_to_spice_node=2 && contact3_to_spice_node=3

In the mixed-mode simulation the device is turned-on from the blocking state with a bias of

300V using a constant current pulse of 0.015A applied to gate from the constant current source labeled Ig. The steady state value of the drain current is set to 15A. The .TRAN statement is used to specify a transient analysis and to control the time-stepping. The simulated waveforms for the gate voltage, drain current, and drain voltage are shown in Fig. 11. From these the associated charges can be extracted by integrating the constant gate current over time.

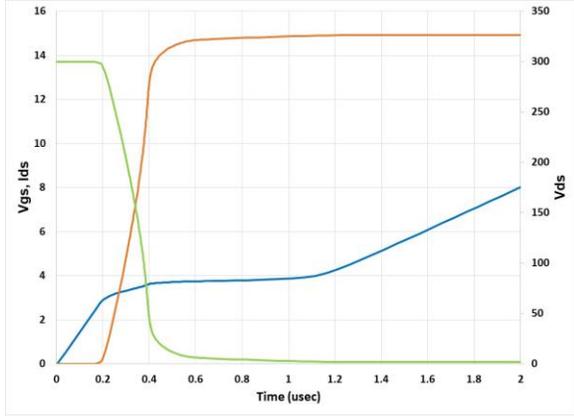


Fig. 11 Superjunction MOSFET Gate Charging Characteristics

F. SJ Capacitances

The capacitances of a generic Superjunction MOSFET are illustrated in Fig. 12. The highly non-linear characteristics are discussed in [4].

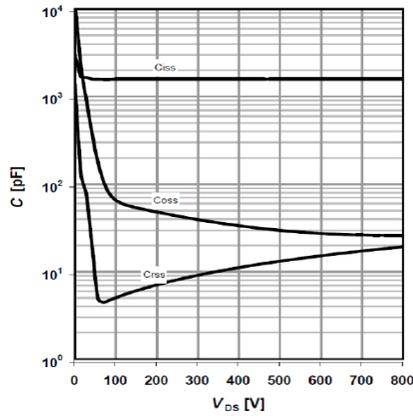


Fig. 12 Typical Superjunction MOSFET Capacitances

The illustrated capacitances are derived from the fundamental terminal capacitances in the usual way.

$$C_{iss} = C_{gs} + C_{gd} \quad (1)$$

$$C_{oss} = C_{ds} + C_{gd} \quad (2)$$

$$C_{rss} = C_{gd} \quad (3)$$

The general methodology for simulating capacitances is described in the APSYS manual [5]. The capacitance simulation is two-step process. First, the DC bias points are calculated from a standard solver file (.sol). This file must contain the statement `more_output ac_data=yes` which retains the AC data for subsequent post-processing. The AC analysis is then performed with an input file using .plt file extension.

The drain-to-source capacitance (Cds) and gate-to-drain capacitance (Cgd) are simulated as function of drain bias using the template files CV_drain.sol, Cgd.plt and Cds.plt. First the CV_drain.sol file is run to generate DC bias points from 0-600V at 10V intervals. The respective .plt files are then used to calculate the terminal capacitances. Similarly, the file CV_gate.sol and Cgs.plt are used to compute the gate-to-source-capacitance, which is independent of drain bias. The output data are stored in appropriately named text files which can be combined according to (1)-(3). The resultant plot is shown in Figure 13. The data of Fig. 13 are qualitatively similar to those of Fig 12 however the two are not identical because of differing device structures.

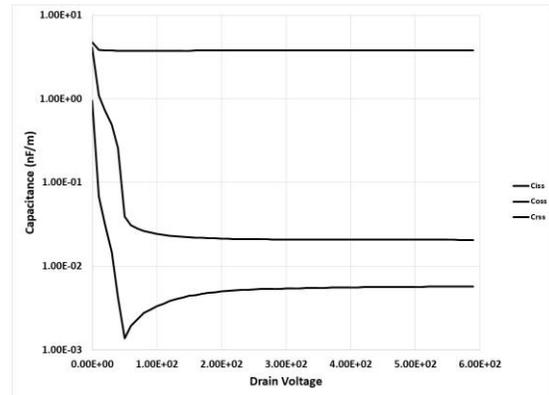


Fig. 13 Simulated Superjunction MOSFET Capacitances

References

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- [2] F. Udrea, G. Deboy, T. Fujihara, "Superjunction Power Devices, History, Development, and Future Prospects", *IEEE Trans.-ED*, Vol 64, No. 3, pp 713-727, March 2017.
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