Application Note

LDMOS Device and Process Simulation

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***Abstract*--A technology template for the process and device simulation of a lateral double-diffused MOS (LDMOS) power transistor using the Crosslight NOVATCAD suite of simulation tools is provided. The example illustrates the use of the process simulation tool CSUPREM to generate a detailed LDMOS device structure. The device structure is imported into the device simulator APSYS and a methodology to simulate the LDMOS electrical characteristics including the drain transfer curves, threshold voltage, on-state resistance, breakdown voltage and electrical safe operating area is demonstrated. Simulation results are displayed and analyzed using the CrosslightView plotting tool.**

I. INTRODUCTION

The lateral double-diffused MOSFET (LDMOS) is one of the most important devices in power integrated circuit applications. A schematic cross-section of the device is shown in Fig. 1.

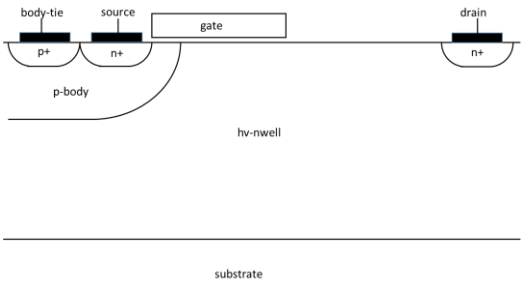

Fig. 1 Generic LDMOS Cross-section.

This example provides a template for performing process and device simulations of LDMOS transistors typical of those found in state-of-the-art BCDMOS (bipolar/CMOS/DMOS) process technologies using shallow-trench isolation [1]. All of the important process steps influencing the LDMOS characteristics are included, however, the additional photo-lithography and implant steps used to form the CMOS and BJT's are omitted.

After the process simulations are completed, a series of device simulations are illustrated including I_d-V_g characteristics, I_d-V_d characteristics, drain breakdown characteristics (BV_{dss}) and electrical safe operating area (SOA).

Author information:
Gary M. Dolny, PhD is a scientific and technical consultant specializing in the areas of analog and power semiconductor devices and technologies. (gary.dolny.us@ieee.org)

II. PROCESS SIMULATION

A. Initial set-up

The initial mesh structure is an important consideration in any process or device simulation. The overall mesh structure is a compromise to achieve a node density sufficient to provide desired simulation accuracy without excessively increasing simulation run time. This example uses approximately 5200 total mesh points, arranged with highest density in the channel regions, and near the junctions, with a correspondingly lower density in other regions of the device. The CSUPREM statements used to generate the initial mesh are shown in Fig. 2. Fig. 3 plots the resultant mesh structure.

```
line x loc=   0.00000  spacing=  0.045
tag=lft
line x loc=   0.80000  spacing=  0.04
line x loc=   1.75000  spacing=  0.02
line x loc=   3.00000  spacing=  0.045
tag=rht


line y loc=   0.00000   spacing=  0.05
tag=top
line y loc=   2.00000   spacing=  0.05
line y loc=   3.00000   spacing=  0.1
line y loc=   5.00000   spacing=  0.2
tag=bot


elimin y.dir xlo=0.00000  xhi=4.0000
ylo=2.00000  yhi5.0000    ntimes=1

region silicon xlo=lft xhi=rht ylo=top
yhi=bot
bound exposed  xlo=lft xhi=rht ylo=top
yhi=top
bound backside xlo=lft xhi=rht ylo=bot
yhi=bot
```

Fig 2 Grid generation statements.

Several parameters are set to control the mesh generation algorithms during diffusion, implantation and deposition. The relatively simple compressive model for oxidation is chosen to minimize run time without significant loss of accuracy since the important oxides are grown on flat surfaces where stress effects are negligible. The corresponding CSUPREM statements are illustrated in Fig. 4.

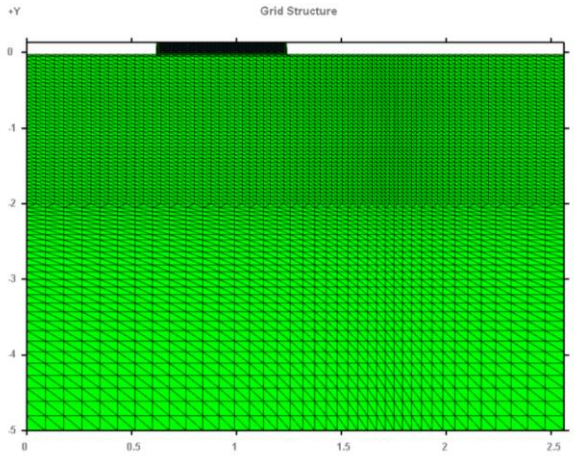

Fig 3 Initial mesh

```
option auto.mesh.implant=t
option auto.mesh.diffuse=t
option deposit.mesh.ratio=0.1

method grid.oxide=0.005
method compress
```

Fig. 4 Parameter settings.

B. Process flow

The process simulation represents a generic LDMOS transistor typical of devices found in BCDMOS technologies with minimum feature sizes 0.18μm. The breakdown voltage is the 30V range therefore an active-gap type structure with no shallow trench isolation in the drift region is employed. The details of the process simulation are shown in Appendix A.

The key process steps simulated are outlined below.

1.) HV N-well implant
2.) HV N-well drive-in
3.) Dual gate oxidation
4.) Polysilicon gate deposition
5.) LDMOS P-body implant and drive in
6.) Source implantation and anneal
7.) Body contact implantation and anneal
8.) Contact formation

A lightly doped p-type starting material is initially defined. The HV-NWELL which is used for the LDMOS drift region and thus controls the device breakdown voltage is then formed by 4 consecutive ion implantation steps of various energies. The main well diffusion is done at 1100^{o}C for 60 minutes in a nitrogen ambient with appropriate screen oxidation and furnace ramp steps illustrated.

Next a sacrificial oxide is grown and subsequently removed to prepare the surface for gate oxidation. The example illustrates a dual-gate oxidation process which is typical of most modern BCDMOS flows. The process forms a relatively thin gate oxide for the CMOS devices and a somewhat thicker oxide for the LDMOS.

First, an initial oxide is grown to a thickness of nominally 10nm. In practice this oxide is removed in areas of the wafer containing the low-voltage CMOS devices and remains in the gate regions of the LDMOS. A second oxidation step which grows nominally 3.5nm of oxide on a bare surface is used to complete the oxidation. The composite thickness of the LDMOS gate oxide is 12nm. Both the initial and final gate oxide thicknesses are extracted and printed into the CSUPREM log file using the PRINT.1D LAYERS statement.

Next the gate polysilicon is deposited and patterned, and the spacer oxide is deposited and etched back. The LDMOS p-body region is formed from a boron ion implantation into the source side of the gate followed by an anneal step to form the LDMOS channel region. The n+ source/drain regions are patterned and implanted, followed by the p+ body tie region. A 15 second rapid thermal anneal to activate the dopants is illustrated. Finally, any remaining oxide is removed in regions which will form the electrical contacts.

The final device structure is stored for subsequent plotting, as shown in Fig. 5, and is exported into a form suitable for use in the APSYS device simulator.

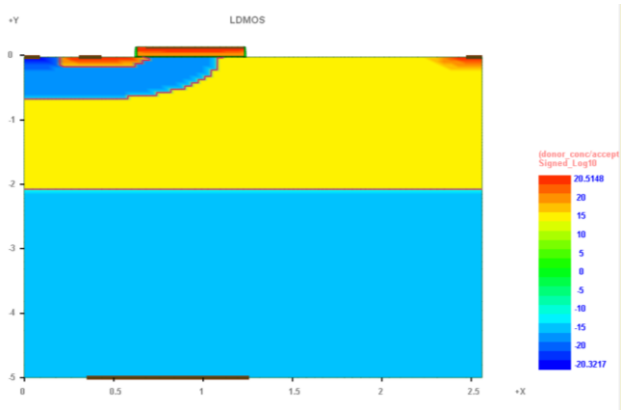

Fig. 5 LDMOS Simulation Structure.

III. SIMULATION OF ELECTRICAL CHARACTERISTICS

The device electrical characteristics are modeled using the APSYS 2-dimensional finite element device simulation tool. Unless otherwise specified the APSYS default physical models are used in these simulations.

A. Basic setup

The basic set-up statements common to all device simulations are shown in Appendix B.

The LDMOS device structure previously generated with CSUPREM export statement is the input structure for the device simulations. The `load_mesh` statement is used to enter the device structure into APSYS. The subsequent `suprem_to_apsys_material` commands maps the CSUPREM materials into the Apsys materials. `suprem_mater` is the original material number in the CSUPREM file, which by default defines SiO2 as material 1, SiN as material 2, Si as material 3, and polysilicon as material 4. `apsys_mater` is the corresponding material number in APSYS. The `load_macro` statements are used to describe the properties of the various materials used in the structure as defined in the materials database. The `suprem_contact` statements are used to define the electrodes on the mesh imported from the process simulator.

The `interface` statement is used to specify the oxide charge, in units of $1/m^2$. The `mobility_xy` statement models the vertical field mobility reduction in the LDMOS channel using the PISCES-2 formulation model while the `impact_okuto_crowell` input statement specifies the Okuta-Crowell formulation for impact ionization.

The statement `newton_par` controls the parameters of the Newton solver used in the software, which can be modified to improve convergence. The scan statements define the bias conditions on each electrode for the various electrical simulations.

B. I-V Simulations

The simulated I_d-V_g characteristics are shown in Fig. 6. Initially the drain voltage is set to 0.1V after which the gate potential is swept from 0V to 5.0V in non-linear increments. The threshold voltage and transconductance are automatically extracted with V_t Extract feature of the CrosslightView visualization tool. The associated scan statements for I_d-V_g simulation are shown in Fig. 6.

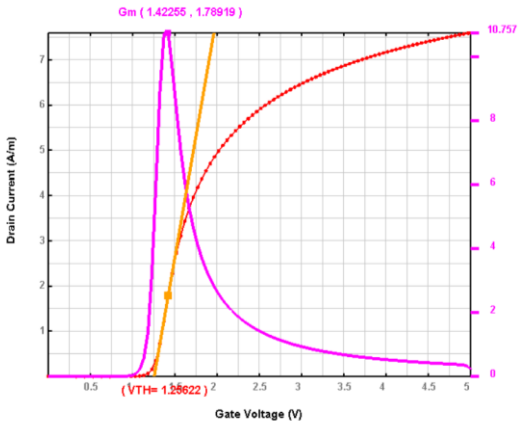

Fig 6 I_d_V_g Characteristic.

```
scan var=voltage_3 value_to=0.1 min_step=1e-
9 max_step=0.05 &&
init_step=0.001

scan var=voltage_2 value_to=4.0 min_step=1e-
9 max_step=0.05 &&
init_step=0.001
```

Fig. 7 Scan statements for Id-Vg simulation.

The simulated I_d-V_d characteristic curves are shown in Fig. 8 for drain bias from 0 to 5 V and gate bias steps from 1V to 5V in 1 volt increments. To generate these characteristics in a single input file a simple re-trace approach is used. Initially the gate voltage is increased to 1V with V_{ds}=0V. The drain bias is then swept to 5V to generate the initial curve. The drain voltage is then retraced back to 0V and the gate voltage is incremented by 1V. The process continues until all curves have been completed. The associated scan statements for I_d-V_d simulation are shown in Fig. 9.

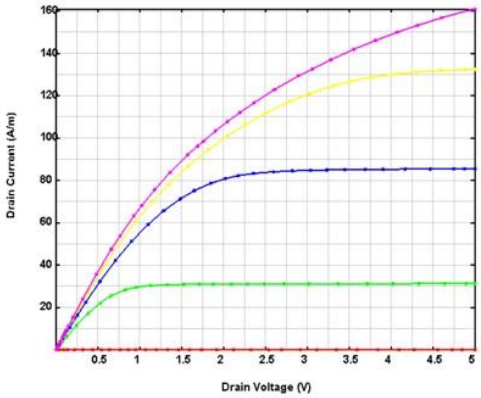

Fig 8 Id-Vd Characteristic Curves.

```
$-----------------------------------------
$ Vg=1.0 Trace
$-----------------------------------------
scan var=voltage_2 value_to=1 &&
min_step=1e-9  max_step=0.5 init_step=0.001

scan var=voltage_3 value_to=5 &&
min_step=1e-6 max_step=2.0 init_step=0.001

scan var=voltage_3 value_to=0 &&
min_step=1e-6 max_step=2.0 init_step=0.001

$-----------------------------------------
$ Vg=2.0 Trace
$-----------------------------------------
scan var=voltage_2 value_to=2 &&
min_step=1e-9 max_step=0.5 init_step=0.001

scan var=voltage_3 value_to=5 &&
min_step=1e-6 max_step=2.0 init_step=0.001

scan var=voltage_3 value_to=0 &&
min_step=1e-6 max_step=2.0 init_step=0.001

$-----------------------------------------
$ Vg=3.0 Trace
$-----------------------------------------
scan var=voltage_2 value_to=3 &&
min_step=1e-9 max_step=0.5 init_step=0.001

scan var=voltage_3 value_to=5 &&
min_step=1e-6 max_step=2.0 init_step=0.001

scan var=voltage_3 value_to=0 &&
min_step=1e-6 max_step=2.0 init_step=0.001


$-----------------------------------------
$ Vg=4.0 Tace
$-----------------------------------------
scan var=voltage_2 value_to=4 &&
min_step=1e-9 max_step=0.5 init_step=0.001

scan var=voltage_3 value_to=5 &&
min_step=1e-6 max_step=2.0 init_step=0.001

scan var=voltage_3 value_to=0 &&
min_step=1e-6 max_step=2.0 init_step=0.001

$-----------------------------------------
$ Vg=5.0 Trace
$-----------------------------------------
scan var=voltage_2 value_to=5 &&
min_step=1e-9 max_step=0.5 init_step=0.001

scan var=voltage_3 value_to=5 &&
min_step=1e-6 max_step=2.0 init_step=0.001
```

Fig 9 Id-Vd scan statements.

The calculation of the LDMOS on-state resistance is similar to the drain characteristic curves. The gate voltage is first raised to the desired value. The drain voltage is then swept to 0.1V to ensure the device remains in the linear region of operation. The-on state resistance is extracted from the inverse slope of the resultant curve shown in Fig. 10. The appropriate scan statements are summarized in Fig. 11.

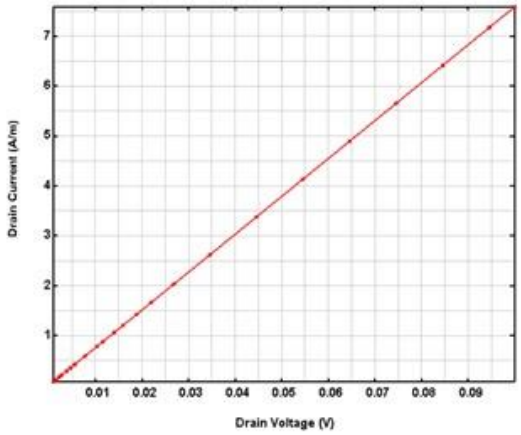

Fig. 10 R_{dson} characteristic.

```
scan var=voltage_2 value_to=5 min_step=1e-9
max_step=0.5 &&
```

```
init_step=0.001

scan var=voltage_3 value_to=0.1 min_step=1e-
9 max_step=0.01 &&
init_step=0.001
```

Fig. 11 Scan statements for on-state resistance.

The drain breakdown voltage characteristics are shown in Fig. 12. The gate voltage is held at 0V while the drain potential is swept positive. The target value for the drain voltage scan is set large compared to the expected breakdown voltage. Once avalanche breakdown initiates, large changes in drain voltage current are produced by small changes in drain voltage, therefore the minimum step step size must be chosen small to accurately capture this effect. In this example the minimum step size is set to 1 micro-volt. The simulation uses the `auto_finish` and `auto_until` commands to stop the calculation when the drain current density reached 10^{-2}A/m. The associated scan statements for the BV_{dss} simulation are shown in Fig. 13.

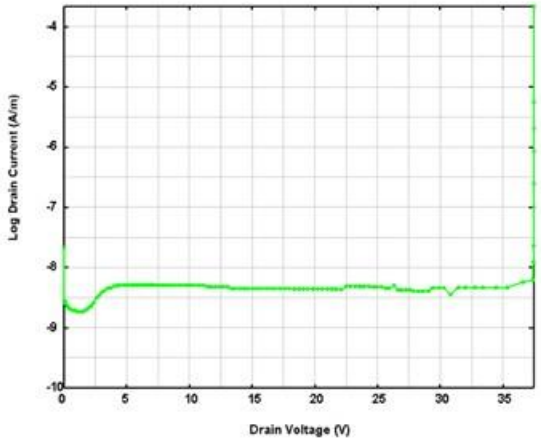

Fig. 12 BV_{dss} Characteristic.

```
scan var=voltage_3 value_to=300 &&
min_step=1e-6 max_step=2.0 &&
auto_finish=current_3 auto_until=1e-2 &&
auto_condition=above &&
init_step=1e-5 var2=time value2_to=100
```

Fig. 13 Scan statement for generating BV_{dss} characteristic.

The electrical safe operating area (SOA) of an LDMOS transistor is defined as the set of voltage and current conditions over which the device can operate without failure in the absence of thermal effects. It is limited by the snapback of the device I_{ds}-V_{ds} characteristic at V_{gs}=0.0V caused by the activation of the parasitic n-p-n bipolar transistor present in the LDMOS structure. The snapback phenomena results in a negative resistance characteristic in the I_d-V_d curve as shown in Fig. 14. This situation can lead to simulator convergence problems since the drain current is a multi-valued function of the drain voltage.

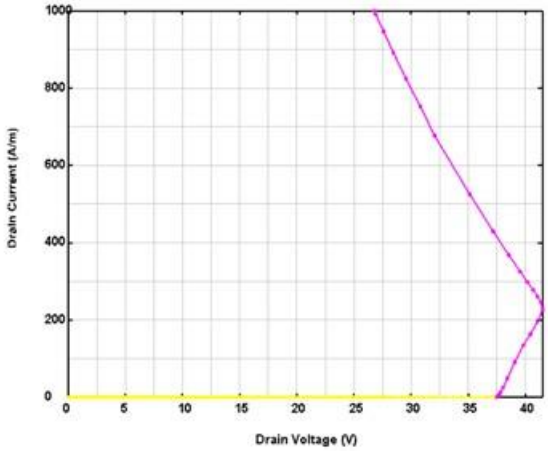

Fig 14 LDMOS SOA Characteristic. The initial voltage scan is shown in gold. The continuing scan for the current boundary conditions is shown in violet.

The scan statements used to generate the SOA characteristic are shown in Fig. 15. They are similar to the BV_{dss} characteristic through the initiation of impact ionization. Instead of halting the simulation the simulation when a specified current density is reached, the simulator switches to a current boundary condition to complete the simulation of the negative resistance portion of the curve.

```
scan var=voltage_3 value_to=300 &&
min_step=1e-6 max_step=2.0 &&
auto_finish=current_3 auto_until=1e-2 &&
auto_condition=above &&
init_step=1e-5 var2=time value2_to=100
scan var=current_3 value_to=1e3  &&
init_step=1.1e-8 min_step=1.e-9  &&
max_step=1.e4
```

Fig 15 Scan statement for generating SOA characteristic.

REFERRENCES

[1] Chou et. al., "0.18um BCD Technology Platform with Best-in-Class LDMOS from 6 V to 70 V," *Proceedings of ISPSD 2012, pp 401-404.*

Appendix A –LDMOS Process Flow

```
#-----------------------------------------
##      Initialize silicon
#-----------------------------------------

init boron conc=3.3e14 orient=100

#-----------------------------------------
#       Screen oxide for HVNW 10nm
#-----------------------------------------

deposit oxide thick=0.01
struct  outf=01ff_screen_hvnw.str

#-----------------------------------------
#       HV-nwell Implant
#-----------------------------------------

implant phosphor dose=0.4e12 energy=150
angle=0 rotation=0
implant phosphor dose=0.4e12 energy=350
angle=0 rotation=0
implant phosphor dose=0.4e12 energy=550
angle=0 rotation=0
implant phosphor dose=0.4e12 energy=750
angle=0 rotation=0
etch    photoresist all

#-----------------------------------------
#       HV-nwell DRIVE-IN
#-----------------------------------------

diffuse time=27  temp=800   dryo2
diffuse time=40  temp=800   final_temp=1100
nitrogen
diffuse time=60  temp=1100  nitrogen
diffuse time=60  temp=1100  final_temp=800
nitrogen
diffuse time=15  temp=800   nitrogen

structure outfile=02ff_hvnw_drive.str

#-----------------------------------------
#       Pad oxide 50 nm
#-----------------------------------------

diffuse time=27 temp=800  dryo2
diffuse time=27 temp=800  final_temp=1000
dryo2

diffuse time=49 temp=1000 dryo2
diffuse time=05 temp=1000 nitrogen
diffuse time=40 temp=1000 final_temp=800
nitrogen

diffuse time=15 temp=800  nitrogen
struct outf=03ff_STI_pad.str

#-----------------------------------------
##  STI Planarization
#-----------------------------------------

etch oxide start x=-1.0 y=-5
etch continue x=-1.0 y=-0.047
etch continue x=5 y=-0.047
etch done x=5 y=-5

etch nitride all


etch oxide start x=-1.0 y=-5
etch continue x=-1.0 y=0.019
etch continue x=5 y=0.019
etch done x=5 y=-5


struct outf=07ff_STI_planarize.str

#-----------------------------------------
##  Sac ox 10nm
#-----------------------------------------

diffuse time=10 temp=800 nitrogen
diffuse time=20 temp=800 final_temp=900
nitrogen
diffuse time=20 temp=900 dryo2
diffuse time=10 temp=900 nitrogen
diffuse time=20 temp=900 final_temp=800
nitrogen


struct outf=08ff_sac_ox.str


#-----------------------------------------
##  Sac Oxide strip
#-----------------------------------------

etch oxide thick=0.01 dry

struct outf=08bff_sac_ox_strip.str

#-----------------------------------------
-
##  HV Gate ox 12 nm total after both gates
#-----------------------------------------

diffuse time=10 temp=800 nitrogen
diffuse time=30 temp=800 final_temp=950
nitrogen
diffuse time=16 temp=925 dryo2
diffuse time=10 temp=950 nitrogen
diffuse time=30 temp=950 final_temp=800
nitrogen
select z=phosphorus
print.1d layers x.value=1.5

struct outf=08ff_HV_gate_ox.str
#-----------------------------------------
##  LV Gate ox 3.5 nm
#-----------------------------------------

diffuse time=10 temp=800 nitrogen
diffuse time=15 temp=800 dryo2
diffuse time=20 temp=800 nitrogen

select z=phosphorus
print.1d layers x.value=1.5
```

```
struct outf=09ff_total_gate_ox.str

#-----------------------------------------
#       Poly Deposition/Pattern
#-----------------------------------------

#deposit poly thick=0.500 meshlayer=10
arsenic conc=1.0e20
deposit poly thick=0.15 meshlayer=10 arsenic
conc=5.0e20
mask x1.from=0.63 x1.to=1.23 thick=1.1
etch poly dry thick= 0.25
etch oxide dry thick=0.02
etch photoresist all

struct outf=10ff_Poly.str

#-----------------------------------------
#       Gate Seal Oxidation 4nm
#-----------------------------------------

method grid.oxide=0.005 viscous
diffuse time=10 temp=800 nitrogen
diffuse time=21 temp=800 dryo2
diffuse time=20 temp=800 nitrogen

struct outf=11ff_gate_seal.str

#-----------------------------------------
#       Pbody implant
#-----------------------------------------

deposit photoresist thick=1.0
etch photoresist left p1.x=0.62
struct outf=11bff_body_photo.str
implant boron dose=7e13 energy=25 angle=0
rotation=0
etch photoresist all

struct outf=11bff_body_imp.str

#-----------------------------------------
#       Pbody anneal
#-----------------------------------------
method compress
diffuse time=10 temp=800 nitrogen
diffuse time=50 temp=800 final_temp=1050
nitrogen
diffuse time=35 temp=1050 nitrogen
diffuse time=50 temp=1050 final_temp=800
nitrogen

#-----------------------------------------
#       Spacer
#-----------------------------------------

deposit nitride thick=0.01 divisions=5
etch nitride thick=0.011 dry

#-----------------------------------------
#       Measure oxide thickness
#-----------------------------------------

select z=phosphorus
print.1d layers x.value=1.5

struct outf=12ff_LDD_spacer.str

#-----------------------------------------
#       N+ Source Drain
#-----------------------------------------

deposit photoresist thick=1

etch photoresist start x=0.18 y=-5
etch continue x=0.18 y=5
etch continue x=1.23 y=5
etch done x=1.23 y=-5

etch photoresist start x=2.38 y=-5
etch continue x=2.38 y=5
etch continue x=3.8 y=5
etch done x=3.8 y=-5

implant arsenic dose=3e15 energy=60 angle=0
rotation=0
structure outf=13ff_source_photo.str
etch photoresist all

#-----------------------------------------
#       P+ Source Drain
#-----------------------------------------

deposit photoresist thick=1

etch photoresist left p1.x=0.18

implant bf2 dose=2e15 energy=20

structure outf=14ff_pplus_photo.str

etch photoresist all

#-----------------------------------------
#        RTA
#-----------------------------------------

diffuse time=0.16 temp=1020 nitrogen
structure outf=15ff_source_drain.str

#-----------------------------------------
#        Contact Etch
#-----------------------------------------
etch oxide left  p1.x=0.55
etch oxide right p1.x=2.3

export outf=ldmos.aps xpsize=0.001
structure outf=16ff_contact.str
```

Appendix B Common Simulation Setup Statements

```
begin

convention positive_current_flow=inward

load_mesh mesh_inf=ldmos.aps
suprem_import=yes
output sol_outf=outfile.out

suprem_to_apsys_material suprem_mater=3
apsys_mater=1
suprem_to_apsys_material suprem_mater=1
apsys_mater=2
suprem_to_apsys_material suprem_mater=4
apsys_mater=3
suprem_to_apsys_material suprem_mater=2
apsys_mater=4

suprem_property user_material_mapping = yes

load_macro name= si mater= 1
load_macro name= sio2 mater= 2
load_macro name= poly mater= 3
load_macro name=sin mater=4


$ Contact Definitions
$ Source=1
$ Gate=2
$ Drain=3
$ P-Body=4
$ Substrate=5

suprem_contact num=1 xrange=(0.15 0.55)
yrange=(-9999.000000 &&
9999.000000) touch_mater=1 side=upper

suprem_contact num=2 xrange=(0.65 1.2)
yrange=(0.05 0.1) &&
touch_mater=3 side=within

suprem_contact num=3 xrange=(2.30 10.00)
yrange=(-9999.000000 &&
9999.000000) touch_mater=1 side=upper

suprem_contact num=4 xrange=(0.00 0.12)
yrange=(-9999.000000 &&
9999.000000) touch_mater=1 side=upper

suprem_contact num=5 xrange=(0.30 1.30)
yrange=(-9999.000000 &&
9999.000000) touch_mater=1 side=lower


contact num=1
contact num=2
contact num=3
contact num=4
contact num=5

interface model=charge &&
within_y=(-0.1, 0.1) &&
within_x=(1.5, 2.5) &&
fix_charge=5e14

mobility_xy elec_field_model=intel1
hole_field_model=intel1

impact_okuto_crowell mater=1
impact_okuto_crowell mater=2
impact_okuto_crowell mater=3
impact_okuto_crowell mater=4



more_output space_charge=yes
impact_ionization=yes ac_data=no &&
 elec_mobility=yes hole_mobility=yes



newton_par damping_step=2. var_tol=1.e-3
res_tol=1.e-3 &&
  max_iter=50 opt_iter=15 stop_iter=15

equilibrium


newton_par damping_step=8. var_tol=1.e-2
res_tol=1.e-2 &&
  max_iter=50 opt_iter=15 stop_iter=15

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
```