Application Note

IGBT Simulation and Analysis

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***Abstract*--A technology template for the simulation of the Insulated Gate Bipolar Transistor (IGBT) using the Crosslight NovaTCAD suite of simulation tools is provided. The example illustrates the use of the process simulation tool CSUPREM to generate the basic device structure. This structure is then imported into the device simulator APSYS for the electrical simulations. A methodology to simulate and optimize the key tradeoffs between breakdown voltage, on-state voltage drop and switching speed is demonstrated. The CrosslightView visualization tool is used to display and analyze the results as well as generate suitable text files for post processing and analysis.**

I. INTRODUCTION

The insulated gate bipolar transistor is a semiconductor power device that combines the high input impedance and ease of gate drive of a MOS structure with the high output current capability of a bipolar transistor. Since its invention in 1982 by Becke and Wheatley [1] the IGBT has undergone rapid development and has become the device of choice for medium and high power applications. In 2019 the worldwide market for IGBTs is estimated to be over $100 million US. The market is expected to grow at a CAGR of roughly 6.4% over the next five years and reach $140 million US by 2024 [2]. Key application areas for the IGBT include industrial motor drives, consumer appliances, automotive, renewable energy and traction.

This market growth has been achieved through continuous improvement in IGBT design. In order to properly understand and optimize these devices, fast and accurate TCAD modeling is essential. This application note presents template files useful for the analysis, design and optimization of IGBT devices using the Crosslight NovaTCAD framework. CSUPREM is used to generate the device structure from the basic process sequence. This is imported into the APSYS device simulator for the electrical simulations. Template files for simulating device breakdown voltage, on-state characteristics, and switching characteristics are provided.

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II. PROCESS SIMULATION

A typical IGBT cross-section is shown in Fig. 1a. A close up of the surface region is shown in Fig. 1b. This structure is representative of a planar punch-through IGBT design. The width of the half-cell is 12 μm. The p-well depth is 1.5μm. The n- epitaxial region is ~55 μm thick with a doping of 2.1×10^{14} cm^{-3}. The n-buffer is ~5 μm thick with an average doping of $3 \times 10^{17} cm^{-3}$.

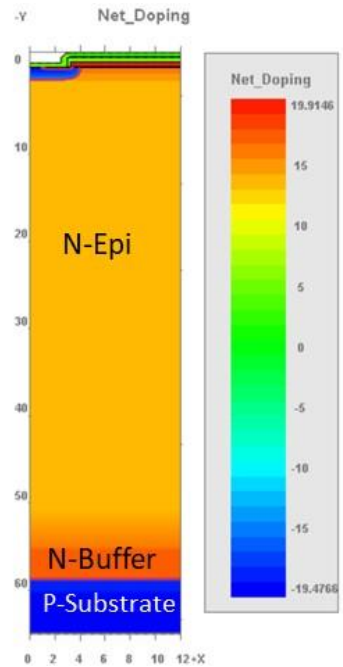

Fig. 1a IGBT Cross-Section

The details of the process simulation are given in the template files. The key process steps simulated are outlined below.

1.) N-epitaxial growth
2.) JFET Implant
3.) Gate oxidation
4.) Polysilicon gate deposition
5.) P-body implant and drive in
6.) Source implantation and anneal
7.) Body contact implantation and anneal
8.) Contact formation
9.) Metal deposition

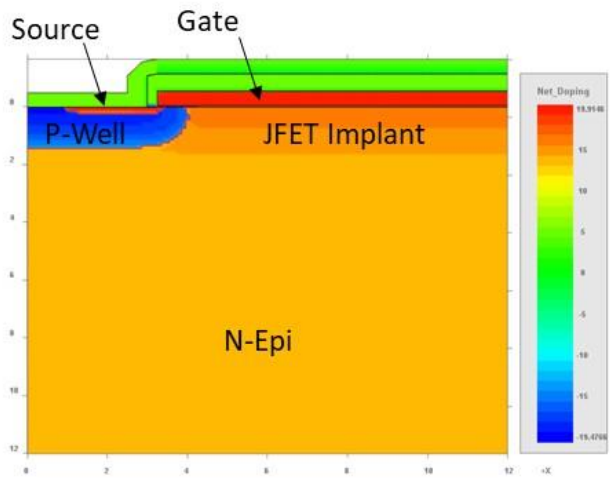

Fig. 1b IGBT surface region

The initial set of CSUPREM statements

```
define @Wp 3.0
define @Wn 9.0
define @Tepi 60
define @Tbuf 5
define @Nd 2.1E14
define @Nbuf 3.0E17
```

specify the values of the important device parameters defined above. Wp is the width of the p-well mask opening while Wn is the distance of the n-epi layer between the p-well and the device symmetry line. The half-cell width is therefore Wn+Wp.

The device structure and initial mesh are defined in the statements

```
line x loc=0
line x loc=@Wp
line x loc=@Wp+@Wn

line y loc=@Tepi
line y loc=@Tepi+5.0
```

Tepi is the total epitaxial layer thickness including the buffer layer. The top of the substrate region is defined at depth of Tepi so that after epitaxial growth the device surface is located at x=0. The n-type buffer layer is initially specified with doping concentration and thickness defined by @Nbuf and @Tbuf respectively. This is followed by the growth of the main epitaxial layer of thickness @Tepi and doping concentration @Nepi. A 60 nm gate oxide is thermally grown followed by the deposition and patterning of the polysilicon gate.

The p-well implant is aligned to edge of the gate polysilicon, followed by the source and p+ body implants, activations and metal deposition. A horizontal cutline of the dopant profile through the channel region is shown in Fig. 2 and the vertical doping through the center of the p-well is shown in Fig. 3.

III. DEVICE SIMULATION

The device electrical characteristics are simulated using the APSYS 2-dimensional finite element device simulation tool. All example files utilize the Lombardi Model for vertical field-dependent mobility and the Chynoweth model for impact ionization. This is done with the statements

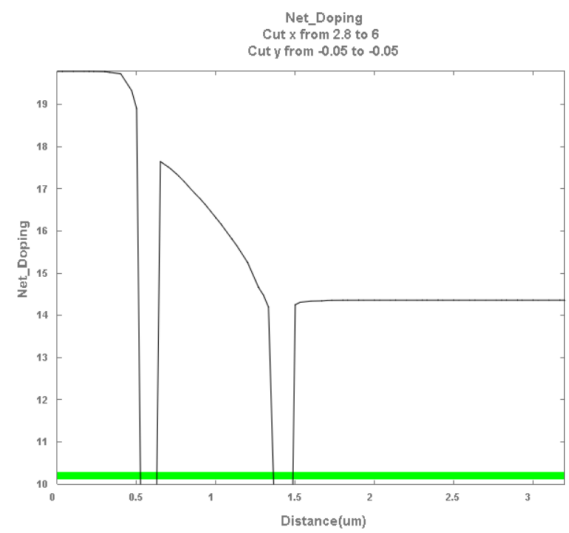

Fig. 2 Simulated doping through channel region

```
mobility_xy
elec_field_model=lombardi &&
hole_field_model=lombardi

impact_chynoweth mater=1
impact_chynoweth mater=2
impact_chynoweth mater=3
impact_chynoweth mater=4
```

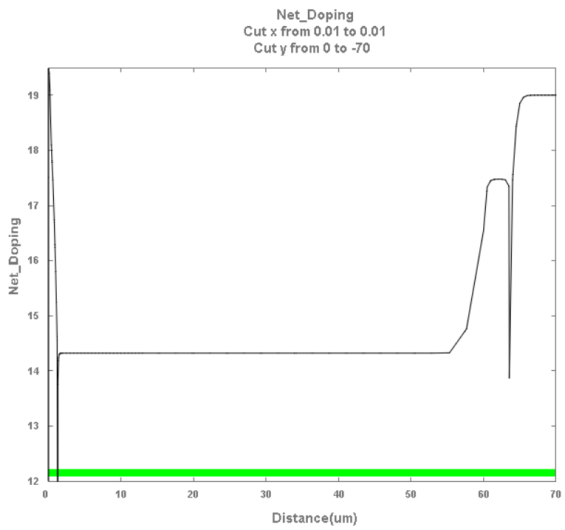

Fig. 3 Doping profile through p-well/epi

The statement

```
Interface model=charge
within_y=(-0.1, 0.1) within_x=(0,
9) fix_charge=5e14
```

specifies the fixed charge at the Si/SiO2 interface, where the units of charge are m^{-2}.

Because the IGBT is a minority-carrier device, the minority carrier lifetime is an important parameter in determining the trade-off between switching speed and on-state conduction losses. Lifetime control techniques such as heavy-metal diffusion or electron irradiation are commonly used to reduce minority-carrier lifetime and thus speed-up recombination time. However, these lifetime control methods increase the on-state voltage drop by reducing the gain of the PNP.

The statements

```
lifetime_n value=100e-9 mater=1
lifetime_p value=100e-9 mater=1
```

are used to specify the electron and hole lifetimes respectively.

In all example files the device area is specified to be 0.1 cm^2 using the statements

```
3d_solution_method skip_fv_data=yes
z_structure single_plane_zdim=8.33E5
```

Unless otherwise specified the APSYS default physical models are used in these simulations. Complete listings of the APSYS input files are provided in the templates.

A. BVces Simulation

The collector-to emitter breakdown voltage (BVces) is the minimum off–state forward blocking voltage guaranteed over the entire IGBT operating temperature range. BVces is specified with the gate terminal tied to the emitter with a collector current sufficiently large to force the device into avalanche breakdown, typically 250 to 500 μA depending on area.

Fig 4 illustrates the equipotential contours of the device at breakdown. The simulated breakdown voltage of 711V of Fig. 4 provides adequate design margin to the commonly encountered 650V maximum rating specified for commercial devices. Fig 5 shows a one-dimensional cutline of the electric field at breakdown through the center of the device.

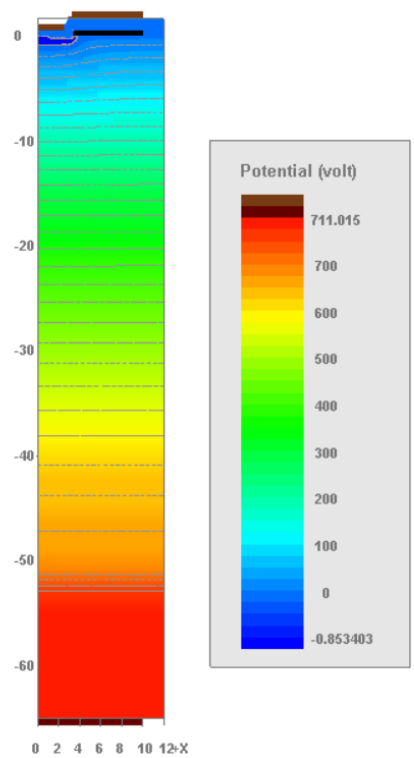

Fig. 4 Equipotential profiles at breakdown

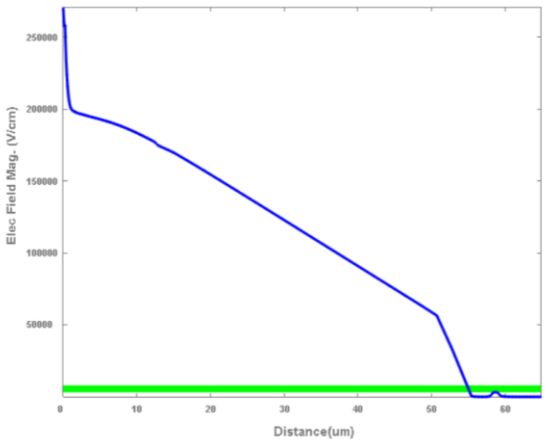

Fig. 5 Electric field at breakdown

B. Id-Vg Characteristics

The gate-to-emitter threshold voltage defines the gate to emitter voltage required for a specified amount of collector current to flow. The current flow depends on device area and is typically in the range of 250 μA. The current is specified for the conditions Vge=Vce.

The simulated Ic-Vg characteristics are shown in Fig. 6 at 25ºC and 125ºC. The threshold voltage at 250 μA are 3.9V and 3.3V respectively. The IGBT simulation shows the expected negative temperature coefficient of threshold voltage.

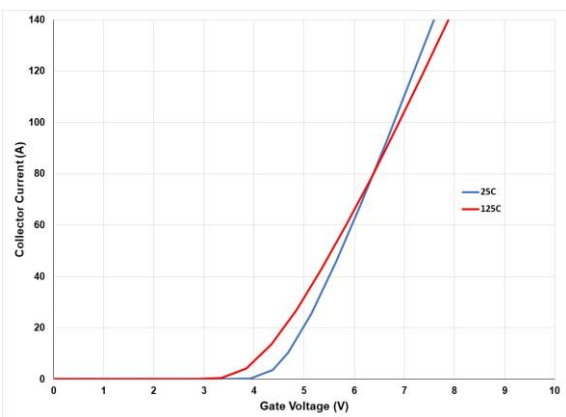

Fig. 6 IGBT Threshold Voltage

C. Vce(sat) Simulation

Vce(sat) is defined as voltage drop between collector and emitter for a specified value of gate voltage and collector current density. This is a crucial parameter since it determines the conduction losses of the device. Typical simulation plots are shown in Fig. 7 for three different values of carrier lifetime. Note that simulations do not account for the additional voltage drop associated with the series resistance of the substrate region.

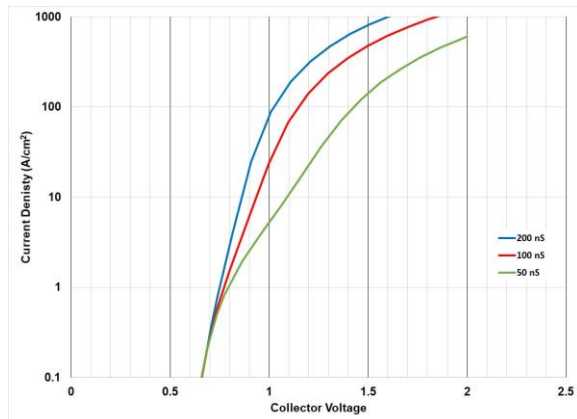

Fig. 7 Vce(sat) simulations

Fig. 7 shows that the Vce(sat) increases as the carrier lifetime decreases. This can be understood with the aid of plots of the electron distributions as obtained from the simulation data using the CrosslightView visualization tool.

The analysis follows the methodology described by Nakagawa [3]. The IGBT structure can be considered to be composed of a pnp transistor region and a pin diode region as shown in Fig. 8.

Fig. 9 shows the electron concentration at the center of the pin region and the center of the pnp region at 100 A/cm^2 for each of the three carrier lifetimes considered. The plots were obtained from CrosslightView by taking one dimensional cutlines of the electron distribution at the appropriate locations in the device.

In Fig. 9, in the pnp region, the electron concentration goes to zero near p-well/n-epi junction because the junction is reverse biased. The electron distribution increases exponentially toward the collector side. In the pin region, the electron concentration near the surface increases

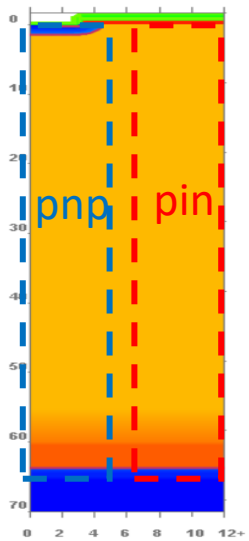

Fig. 8 IGBT illustrating pnp and pin regions

due to the presence of the accumulation layer that forms in the n-epi under the positively biased gate. The carrier density is high near both surface and near the emitter.

Fig. 9 clearly shows the reduction in the number of electrons as the carrier lifetime is reduced. The

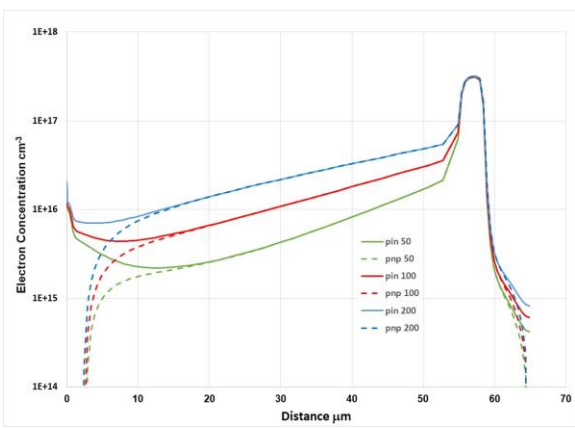

Fig 9. Electron concentration vs distance for various carrier lifetimes

reduced number of free carriers is responsible for the increased on-state voltage as carrier lifetime is reduced as shown in Fig. 7.

D. Switching Simulation

The double pulse switching test is the standard method for measuring the switching parameters of power devices. A generic test circuit is shown in Fig. 10.

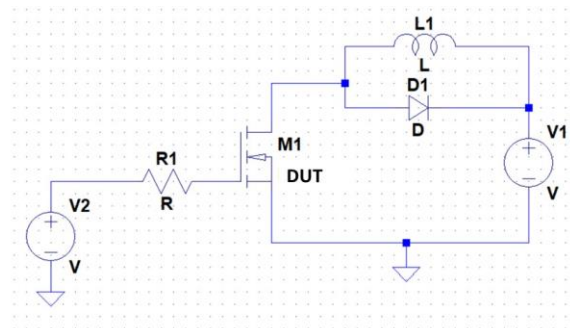

Fig 10. Double pulse switching circuit

The test consists of two gate pulses. The first gate pulse establishes the desired test current in the inductor. At the turn-off of the first pulse the fall time of the test device is measured. The initial current now flows through the inductor and the freewheeling diode. Due to the high inductance and short turn-off period the current remains almost constant during this time. The turn-on of the second pulse transfers the load current into the IGBT. The reverse recovery of the freewheeling diode during this phase results in current overshoot. The risetime of the device under test is measured during the leading edge of this pulse.

The mixed-mode feature of the APSYS simulation tool is used to simulate the IGBT double-pulse switching test. In this mode, the TCAD device is defined inside a SPICE circuit file using a placeholder element, with the drift-diffusion model replacing the usual SPICE compact model of the device during the full mixed-mode simulation. The simulation results are shown in Fig 11.

The important switching parameters such as fall time, rise time, turn-on delay, and switching energy can be extracted from Fig. 11 using the standard definitions [4].

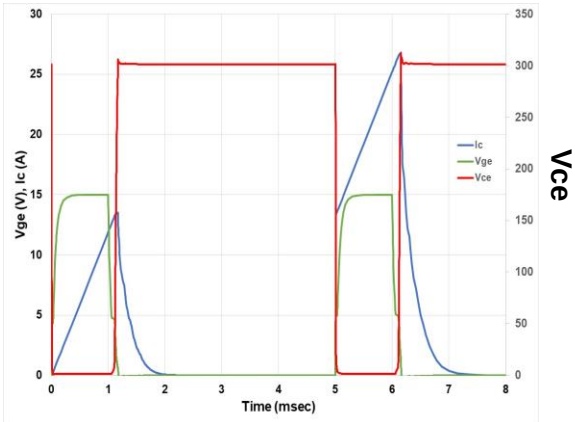

Fig. 11 Double pulse switching simulation Minority carrier lifetime= 100 nsec

Further insight into the dynamic behavior can be observed from plots of the IGBT internal carrier distributions during switching. These plots are obtained by capturing the device data at various times during the switching transient using the command

```
scan var=time value_to=2.5e-6
init_step=1e-10 min_step=1e-14
max_step=1e-7 print_step=0.1e-6
```

The statement `print_step=0.1e-6` captures device data every 100 nS during the switching cycle for later plotting.

The IGBT minority carrier distributions at various times during the switching cycle are shown in Fig. 12.

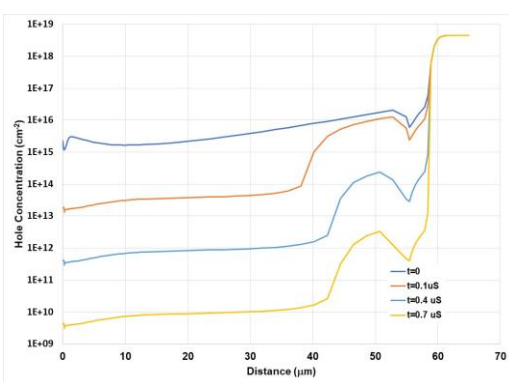

Fig 12. Minority carrier distribution during switching

During switching the emitter/n-epi junction becomes reverse biased and a depletion layer forms near the junction. As time progresses and the collector voltage rises, the depletion layer expands. The expanding depletion moves toward the collector and sweeps out the minority holes into the emitter. Once the depletion reaches its maximum width, limited by the presence of the buffer layer, current flows by pnp action until the remaining carriers near the n-buffer recombine.

E. Vcs(sat) vs Switching Tradeoff

The trade-off between conduction loss and switching speed is an important IGBT figure of merit. For a given device design, as switching time improves typically the Vce(sat) and hence conduction losses increase. The tradeoff can be analyzed by performing multiple simulations of Vce and switching with varying carrier lifetime then plotting the resultant Vce(sat) vs fall time as shown in Fig. 13.

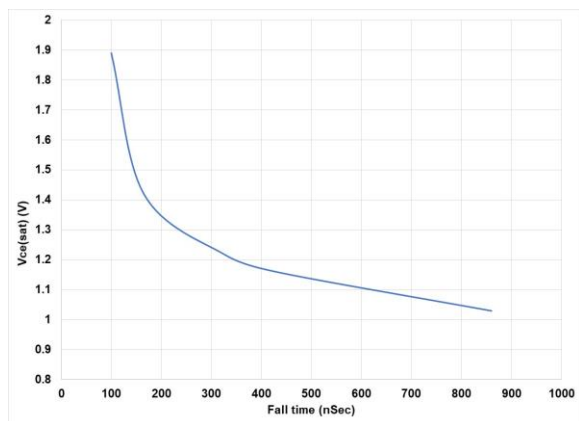

Fig 13. IGBT fall time vs Vce tradeoff

IV. SUMMARY

Template files for the simulation of the Insulated Gate Bipolar Transistor (IGBT) using the Crosslight NovaTCAD suite of simulation tools are provided. The examples illustrate the use of both process and device simulation to analyze and optimize IGBT designs. A methodology to simulate and optimize the key tradeoffs between breakdown voltage, on-state voltage drop and switching speed has been demonstrated.

References

[1] Becke HW, Wheatley Jr CF: "Power MOSFET with an anode region", United States Patent Nr. 4,364,073, Dec. 14, 1982 (filed March 25, 1980).

[2] https://www.marketwatch.com/press-release/global-igbt-market-2019-by-manufacturers-regions-type-and-application-forecast-to-2024-2019-04-01

[3] http://nakagawa-consult.main.jp/FC2/AdvancedPowerDevices.pdf

[4] *Reading On Semiconductor Data Sheets*, ON Semiconductor Application Note AND9068/D