Application Note

Si-JBS Diode Simulation

Updated 2019.01

© Crosslight Software Inc.

***Abstract*— A technology template for the simulation of a Silicon Junction Barrier Schottky (Si-JBS) diode using the Crosslight NOVATCAD suite of simulation tools is provided. The example illustrates the use of the process simulation tool CSUPREM to generate the basic device structure and simulation grid. The structure is imported into the device simulator APSYS and a methodology to simulate the Si-JBS electrical characteristics including the forward and reverse I-V characteristics is demonstrated.**

I. INTRODUCTION

Schottky barrier rectifiers are important in a wide variety of power switching applications due to their low forward voltage drop and low reverse recovery charge. However, the low barrier height of the Schottky contact can lead to excess leakage current and reduced maximum operating temperature, thus limiting device performance. These problems can be alleviated through the use of the Junction Barrier Schottky (JBS) diode structure.

The JBS diode consists of a surface Schottky barrier, protected by p-n junctions formed in the drift region. Under reverse bias, the depletion regions associated with the p-n junctions expand under the Schottky barrier and are designed to pinch-off at relatively low voltage. The resulting potential barrier then shields the Schottky contact from additional reverse voltage, minimizing Schottky-barrier lowering, thus reducing the reverse leakage current. In addition, the presence of the p+ region improves the diode surge current capability. At sufficiently large forward bias the p+ region begins to inject minority carriers, that can modulate the resistivity of the drift region and thus reduce power dissipation at high current levels.

In order to properly understand and optimize these devices fast and accurate TCAD modeling is essential. This application note presents template files useful for the analysis, design and optimization of JBS diode structures using the Crosslight NOVATCAD framework. CSUPREM is used to generate the device structure from the basic process sequence. This is imported into the APSYS device simulator for the electrical simulations. Template files for simulating device on-resistance and drain breakdown voltage (BV_{dss}) are provided.

II. PROCESS MODELING

A typical JBS diode is described in [1]. A cross-sectional view of a half-cell is shown in Fig. 1.

Author information
Gary M. Dolny, PhD is a scientific and technical consultant specializing in the areas of analog and power semiconductor devices and technologies. (gary.dolny.us@ieee.org)

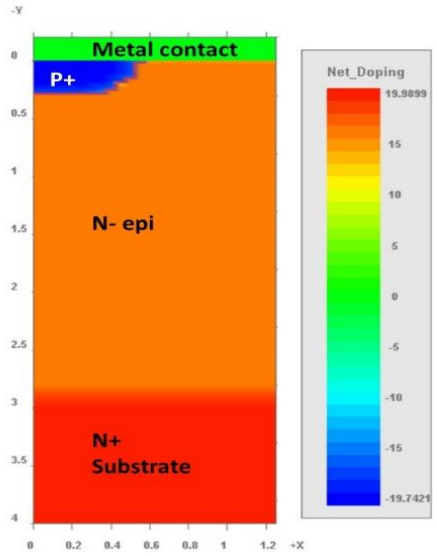

Fig. 1 Schematic cross-section of JBS Rectifier

The device is fabricated on an arsenic doped substrate with doping density of $1x10^{20}$ cm^{-3}. The epitaxial n-type drift region has thickness of 3 μm and a uniform doping of $8x10^{15}$ cm^{-3}. The p+ region is formed from a boron ion implantation with a dose of $1x10^{15}$ cm^{-2} at an energy of 20 keV. A 900° C drive-in step for 30 minutes produces a final p+ junction depth of ~0.3 μm. The spacing between adjacent p+ regions is ~1.5 μm. The structure is completed with the deposition of a metal Schottky contact layer. In the process simulation example, titanium is used as the contact material. However, the selection of the contact material is arbitrary. The properties of any suitable metal system can be simulated by proper choice of the metal workfunction in the subsequent device simulation.

A complete listing of the CSUPREM process simulation file is provided in the template files.

III. DEVICE SIMULATION

The device electrical characteristics are simulated using the APSYS 2-dimensional finite element device simulation tool. Unless otherwise specified the APSYS default physical models are used in these simulations. Complete listings of the APSYS input files are provided in the template files.

A. Simulation setup

The JBS device structure previously generated with the CSUPREM export statement is the input

structure for the device simulations. The `load_mesh` statement is used to enter the device structure into APSYS. The subsequent `suprem_to_apsys_material` commands map the CSUPREM materials into the APSYS materials. `suprem_mater` is the original material number in the CSUPREM file, which by default defines SiO2 as material 1, SiN as material 2, Si as material 3, and polysilicon as material 4 and titanium as material 6. `apsys_mater` is the corresponding material number in APSYS. The `load_macro` statements are used to describe the properties of the various materials used in the structure as defined in the materials database.

The `suprem_contact` statements are used to define the electrodes on the mesh imported from the process simulator.

The properties of the Schottky contact are determined by statements

```
affinity mater=6 value=4.89
no_auto_workfunction mater= 6
```

`affinity` is a passive macro material statement defining the electron affinity (in eV) of the top contact. In metal this value is equal to the work function. This sets the Schottky barrier height through the well-known relationship

$$\phi_b = q(\phi_m - \chi)$$

Wϕ_b is the barrier height, ϕ_m is the metal workfunction (electron affinity of the metal) and χ is the electron affinity of the semiconductor. In the example file the workfunction is set to 4.89 eV. Note that the properties of the Schottky contact are determined by the workfunction specified in the `affinity` statement, and not by the material name specified in CSUPREM. Thus, this example simulates a PtSi Schottky barrier due to the specified workfunction of 4.89 eV.

The `interface` statement is used to specify the oxide charge, in units of m^{-2}. The `mobility_xy` statement models the carrier mobility reduction using the Lombardi model while the `impact_okuto_crowell` input statement specifies the Okuto-Crowell formulation and coefficients for impact ionization.

The statement `newton_par` controls the parameters of the Newton solver used in the software, which can be modified to improve convergence. The scan statements define the bias conditions on each electrode for the various electrical simulations.

B. BV Simulation

Device breakdown voltage characteristics are computed using the `scan` statements shown below.

```
scan var=voltage_2 value_to=2000
min_step=1e-6 max_step=10.0
auto_finish=current_3
auto_until=3e-8
auto_condition=above
init_step=0.001

scan var=current_2 value_to=1e-4
init_step=1.1e-8 min_step=1.0e-9
max_step=1.e4
```

Initially the cathode voltage is swept until a specified avalanche current is reached as defined by the `auto_finish` and `auto_until` statements. After this the simulation switches to a current boundary condition to allow the rest of the I-V curve to be computed. A typical I-V curve at breakdown is shown in Fig. 2, with a simulated breakdown voltage of 55V. Fig. 3 plots the two-dimensional electrostatic potential at breakdown.

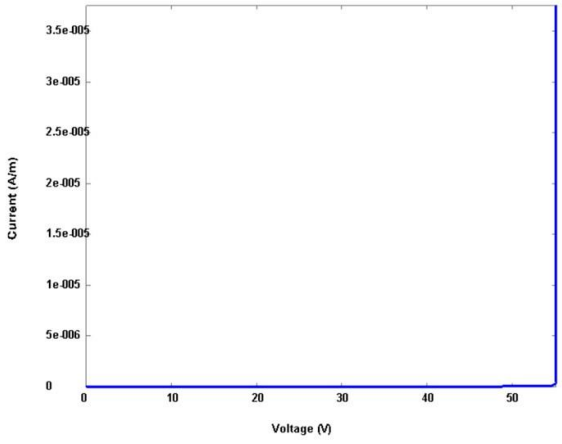

Fig 2. Simulated breakdown characteristic

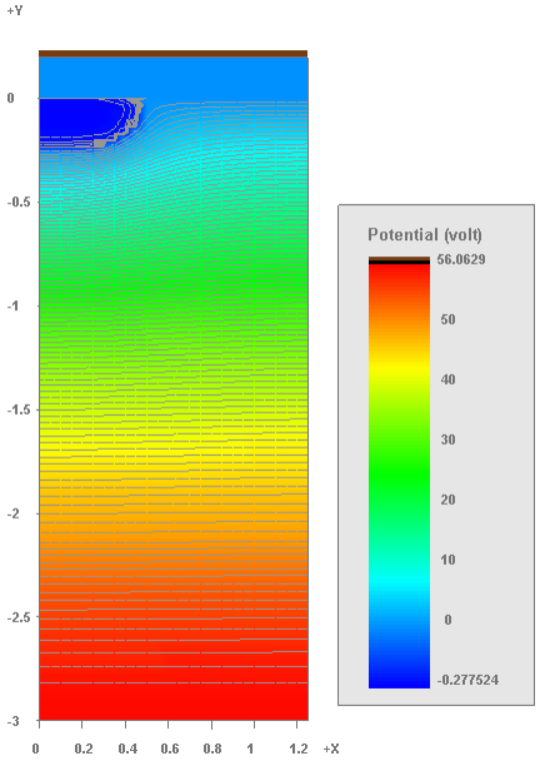

Fig 3. Simulated equipotential lines at breakdown

C. Rdson Simulations

The JBS forward I-V characteristics are simulated using the `scan` statements shown below.

```
scan var=voltage_2 value_to=2.8
min_step=1.0e-6 max_step=0.02 &&
init_step=0.001
```

Contact 2 is the anode contact while contact 1 is the cathode. The simulated forward I-V characteristic is shown in Fig. 4.

Fig. 4 shows the total anode current flowing through the anode contact which consists of current through the surface Schottky region plus current through the p+ region. In some cases, it is useful to separate the two current components. This can be done be splitting the top surface contacts into two separate segments as shown in Fig. 5. One segment contacts the p+ region and another contacts the Schottky barrier. In the example, the p+ contact is defined as contact 1, the top Schottky is defined as contact 2, while the cathode is defined as contact 3. Negative bias is applied to the cathode. The current through each contact can then be plotted independently as shown in Fig. 6. At low bias, the current through the p+ region is many orders of magnitude smaller than the Schottky current. The p+ current becomes larger at higher forward bias consistent with the forward biasing of the p+ regions. Note that the actual forward bias voltage across the p+ region is not identical to the contact voltage due to the high current density combined with series resistance of the epitaxial layer.

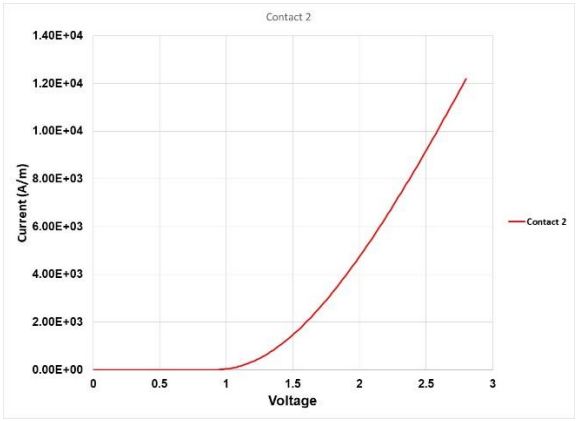

Fig 4. Forward I-V characteristics

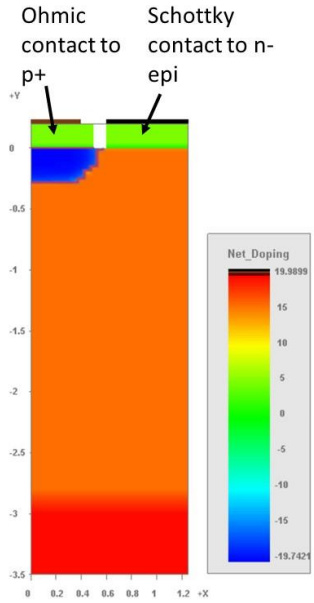

Fig 5. Split contact structure

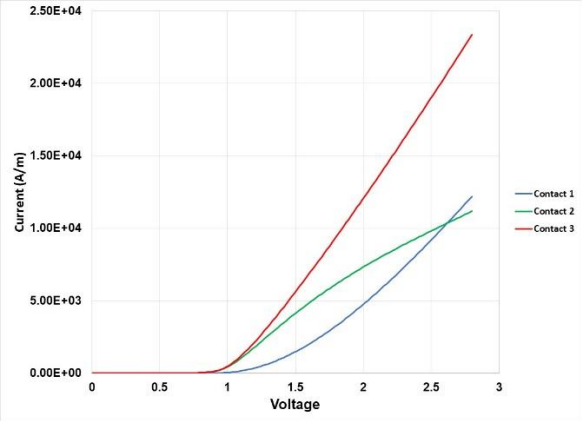

Fig. 6 forward I-V characteristics illustrating total current, p+ component, and Schottky component

Reference

[1] B. J. Baliga, *Advanced Power Rectifier Concepts*. Ney York, NY: Springer, 2009, pp. 39–44.